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QUALITY PROCEDURES FOR VLSI/VHSIC (VERY LARGE SCALE
INTEGRATED AND VERY H. (U) ITT ADVANCED TECHNOLOGY
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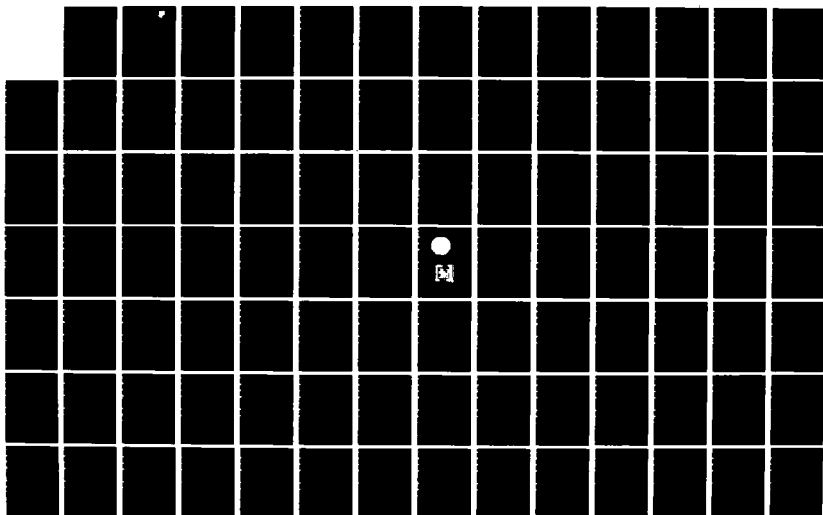
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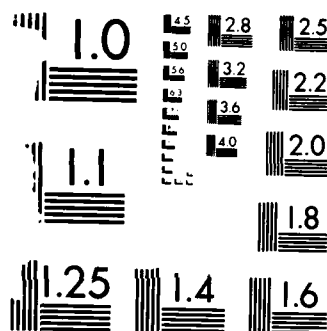
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AD-A164 885

RADC-TR-85-219
Final Technical Report
November 1985

QUALITY PROCEDURES FOR VLSI/VHSIC TYPE DEVICES

ITT Advanced Technology Center

Seymour Cohen, Michael Macari and Steve Yu

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RADC-TR-85-219 has been reviewed and is approved for publication.

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SECURITY CLASSIFICATION OF THIS PAGE

AD-A164885

REPORT DOCUMENTATION PAGE				
1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED (NO FOREIGN NATIONALS)		1b. RESTRICTIVE MARKINGS N/A		
2a. SECURITY CLASSIFICATION AUTHORITY N/A		3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited		
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A				
4. PERFORMING ORGANIZATION REPORT NUMBER(S) N/A		5. MONITORING ORGANIZATION REPORT NUMBER(S) RADC-TR-85-219		
6a. NAME OF PERFORMING ORGANIZATION ITT Advanced Technology Center	6b. OFFICE SYMBOL (if applicable)	7a. NAME OF MONITORING ORGANIZATION Rome Air Development Center (RBRA)		
6c. ADDRESS (City, State, and ZIP Code) 1 Research Drive Shelton CT 06484		7b. ADDRESS (City, State, and ZIP Code) Griffiss AFB NY 13441-5700		
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Rome Air Development Center	8b. OFFICE SYMBOL (if applicable) RBRA	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F30602-83-C-0083		
8c. ADDRESS (City, State, and ZIP Code) Griffiss AFB NY 13441-5700		10. SOURCE OF FUNDING NUMBERS		
		PROGRAM ELEMENT NO	PROJECT NO	TASK NO
		62702F	2338	01
				WORK UNIT ACCESSION NO. S1
11. TITLE (Include Security Classification) QUALITY PROCEDURES FOR VLSI/VHSIC TYPE DEVICES				
12. PERSONAL AUTHOR(S) Seymour Cohen, et al				
13a. TYPE OF REPORT Final	13b. TIME COVERED FROM Sep 83 TO Sep 85	14. DATE OF REPORT (Year, Month, Day) November 1985	15. PAGE COUNT 136	
16. SUPPLEMENTARY NOTATION Approved for distribution to all qualified DTIC users				
17. COSATI CODES		18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)		
FIELD	GROUP	SUB-GROUP		
07	01			
09	03			
		Very Large Scale Integrated and Very High Speed Integrated Circuits, (VLSI/VHSIC) 9		
		Line Certification, 6111 Qualification Procedures (over)		
19. ABSTRACT (Continue on reverse if necessary and identify by block number)				
<p>Procedures for microcircuit screening and qualification to ensure the reliability and uniformity of VLSI/VHSIC devices were prepared on this effort. The use of Process Control Monitors (PCM) and Reliability Evaluation Modules (REM) were incorporated in the procedures. In addition, recommended guidelines for the evaluation of Computed-Aided-Manufacturing (CAM) facilities were generated in this study. A proposed replacement was provided for existing Method 5007 to MIL-STD-883, Wafer Acceptance Procedure which incorporates reliability screening, process quality evaluation, and electrical parameter testing of each wafer in a lot.</p>				
20. DISTRIBUTION/AVAILABILITY OF ABSTRACT <input checked="" type="checkbox"/> UNCLASSIFIED/UNLIMITED <input type="checkbox"/> SAME AS RPT <input type="checkbox"/> DTIC USERS		21. ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED		
22a. NAME OF RESPONSIBLE INDIVIDUAL Peter F. Manno		22b. TELEPHONE (Include Area Code) (315) 330-2922		22c. OFFICE SYMBOL RADC (RBRA)

UNCLASSIFIED

Block 18. Subject Terms (cont'd)

Complex Monolithic Microcircuits (CM²)

Silicon Foundry

Wafer Lot Acceptance

Process Control Monitors (PCM)

Test Strips

Reliability Evaluation Modules (REM)

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EVALUATION

The objective of this effort, which supports RADC TPO 4F.1 Solid State Device Reliability, was to establish optimum cost effective procedures for the certification of process lines and materials and the baselining of processes used in the fabrication of standard and custom Very Large Scale Integrated and Very High Speed Integrated Circuits (VLSI/VHSIC) including those utilizing silicon foundries. The results of this effort will be used to develop baseline documentation to ensure that the necessary controls are in place to guarantee the consistency of product.

As a result of this effort, the following proposed procedures were generated: "Vendor Validation" (A1), "Wafer Acceptance" (A2), "Manufacturer and Line Certification Requirements for VLSI/VHSIC Assembly" (A3), and "Certification Requirements for VLSI Microcircuits Facilities and Lines" (A4). In addition, guidelines for auditing the Computer Aided Manufacturing (CAM) capabilities and process controls of suppliers have been included. The proposed wafer acceptance procedures have been incorporated into draft Test Method 5007.5 to MIL-STD-883, "Test Methods and Procedures for Microelectronics," and will be used for DOD and Industry coordination. Also, the use of Process Control Monitors (test structures), and Reliability Evaluation Modules (REM) were incorporated into this procedure. The proposed new test procedures are considered unique in that they will require the audit/certification of microcircuit manufacturers at the wafer level and will be used for standard and nonstandard parts.

The effort was highly successful in satisfying the above objectives and should result in the generation of the documentation and testing required for the military usage of VLSI/VHSIC. The proposed documents have been presented in a format which will facilitate the transfer to military documents. The information provided will form the basis for revising the appropriate sections of MIL-M-38510, "Microcircuits, General Specification for," and MIL-STD-883 to make them applicable to VLSI/VHSIC devices. Future work will be conducted in establishing the test patterns and testing limits required to implement these procedures.



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Project Engineer

PREFACE

This Final Technical Report was prepared by ITT Advanced Technology Center, Shelton, Connecticut, under Air Force Contract F30602-83-C-0083. The contract was administered under the technical direction of Mr. John P. Farrell and Mr. Peter F. Manno of the Rome Air Development Center, Griffiss Air Force Base, New York.

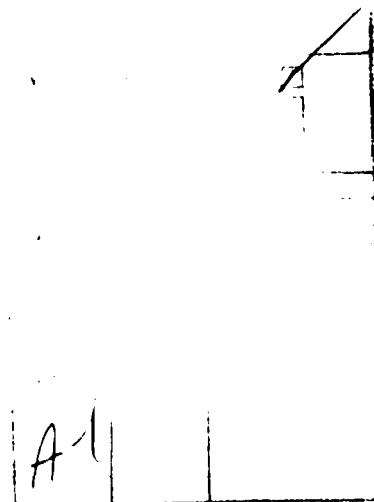
This report covers the work performed from November 1, 1983 to December 31, 1984. Swamy Thangamuthu and Seymour Cohen were the project managers. Michael Macari was responsible for the work on Wafer Lot Acceptance; Steve Yu was responsible for the Wafer Foundry Certification efforts; Don Meyer was responsible for the VHSIC Assembly Certification Procedures. We also wish to acknowledge the contributions of the following:

- o From ITT Advanced Technology Center:
 - o Bud Firth
 - o Anil Kohli
 - o Richard Byrne
- o From ITT Semiconductors:
 - o Joseph Fabula
 - o Al Licata

We also gratefully acknowledge the assistance provided on the program by John Farrell and Peter Manno of RADC, and Ed Hakim, ERADCOM.

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1. INTRODUCTION

- 1.1 Objective. The objective of this program was to develop procedures for validating process lines, processes and materials used in the fabrication of standard and custom VLSI/VHSIC and silicon foundry type devices, to assure that they are adequately baselined and controlled.
- 1.2 Background. Recent revisions of the military specifications for microcircuits (MIL-M-38510F) and test methods (MIL-STD-883C) still reflect the philosophy of assuring device reliability by screening defects, or potential failures, out of a lot at the end of the fabrication cycle. The low volume, high complexity and high costs of VLSI/VHSIC devices make the existing procedures for screening and qualification too expensive and time consuming. As device complexity increases, manufacturers have incorporated computer-aided manufacturing (CAM) techniques in wafer fabrication, test and assembly to achieve the process controls necessary for economic device yields. The use of surrogate devices for process-monitoring and characterization is now a well established practice for VLSI circuit manufacturing. The use of surrogate devices for reliability screening, yield verification and process qualification is currently the subject of various investigations. As part of this contract study, we have proposed quality procedures using surrogate devices for lot acceptance and silicon foundry assessment. We have also utilized the experience gained from the extensive use of CAM facilities at ITT Semiconductors Wafer Fabrication facility (formerly part of ITT's ATC/VLSI Technology Division) to develop guidelines for evaluating the use of CAM in VLSI/VHSIC manufacturing.

2. SUMMARY/DISCUSSION OF PROPOSED PROCEDURES

2.1 Silicon Foundry Validation (Appendix A1). For custom VLSI, the user is also the device designer, rather than the device manufacturer. The design and layout of custom chips, as well as the test programs, are the user's responsibility. The device manufacturer is responsible for design rules and processing. These changing responsibilities have resulted in the establishment of "silicon foundry" type device manufacturers. Today both merchant manufacturers and new ventures specifically established for wafer processing custom circuits are in the silicon foundry business. The custom VLSI device specification must clearly define the individual responsibilities of the silicon foundry and the user/designer. In addition to selecting the wafer manufacturer, the user now has the additional tasks of selecting the technology, correlating test results and resolving responsibilities for yield problems.

Multiple-sourcing requires the designer to evaluate the design rules and processes of several suppliers and design test vehicles as well as the custom arrays, that can be processed successfully by more than one supplier.

The designer's test program organization, combined with the evaluation of test insert chips, must be capable of resolving interface problems between the designer and the foundry. The foundry is responsible for meeting the specified limits on the D.C. test parameters. The functional test, as well as the correctness of the test vectors, are strictly the responsibility of the design activity. The D.C. interface parameters (power supply, inputs/outputs) are the joint responsibility of the designer and the manufacturer.

The proposed foundry validation procedure (Appendix A1) does not attempt to define a standardized test structure for wafer acceptance testing. It does define, for MOS technologies, a minimum set of process and electrical parameters required to determine whether a process (or lot) meets the design requirements. Section 5.4 in the

validation procedure defines the characteristics of the Process Validation Module (PVM) that includes the specified electrical and process validation parameters. It also includes the requirement for a Reliability Evaluation Module (REM), but does not define it.

2.2 Wafer Lot Acceptance (Appendix A2)

2.2.1 Background. The current Wafer Lot Acceptance Procedure, (Method 5007.5, MIL-STD-883C), required for only Class S devices, is basically a physical trait measurement test, which does not address any basic process or electrical parameters. This does not reflect current internal procedures used in the semiconductor industry where "Process Control Monitors" (PCM) or "drop-in" die are used to verify that the process is in specification, regardless of the circuit being manufactured. This drop-in would indicate if the wafer should be tested or scrapped. This procedure will attempt to integrate the use of PCM, test strips and Reliability test structures into the Wafer Lot Acceptance process.

2.2.2 Introduction. The trend in the semiconductor industry is towards automation. The goal is a structured fabrication process where process equipment is controlled by, and returns data to a host computer. The host computer functions include process control, process monitoring, wafer tracking, data analysis and management.

To implement the Wafer Lot Acceptance procedure being proposed, interface of electrical test equipment to a CAM System is considered the optimum approach. This is because a large amount of data (electrical parameters) will be taken and must be reduced to meaningful information. This information will indicate whether a wafer is accepted or rejected. Data management capability is the cornerstone of wafer acceptance.

Another reason for the use of CAM data management is that wafer processing is not totally batch or lot produced. There are steps in fabrication where wafers are processed independently, leading to variations in yield from wafer to wafer in one lot. Therefore, tracking and data collection should be on a wafer basis, rather than a lot basis. It would then be possible for a wafer to be accepted, though other wafers in the same lot were rejected. This condition is common in the fabrication process.

2.2.3 Philosophy. The proposed procedure (Appendix A2) is a totally new Wafer Lot Acceptance method. The new method's philosophy will stress that wafers be evaluated individually, without dependence on the performance of other wafers in that lot. Therefore, the new method would be a Wafer Acceptance Procedure. Secondly, the use of Process Control Monitors (PCM), test strips and Reliability Evaluation Modules (REM) have been incorporated into this procedure. The evaluation of these structures will determine whether the wafer is accepted.

2.2.4 Conditions for Wafer Acceptance. Before a wafer acceptance methodology is instituted in a foundry, the facility must have CAM in operation. The system must have the capability of tracking wafers on an individual basis. Process technicians must be able to retrieve wafer-related information and enter all wafer-related information into the system. Automation of equipment, i.e. CAM system control of process equipment, is not required.

Electrical test equipment, which performs Wafer Acceptance testing, must be interfaced to the CAM. This allows data from Parametric Testers used for measuring Process Control Monitors (PCM), Test Strip and Reliability Evaluation Monitors (REM), and data from Functional Testers, used in CM² testing to be collected by the CAM. This electrical data will be combined with previously collected fabrication data, entered during processing. The CAM system must not only store this data, it must also organize it. That is, it must be able to identify the wafer and where on the wafer the data was collected.

The enormous amount of raw data generated using a Wafer Acceptance procedure would overwhelm those who must utilize it. Therefore, sophisticated data analysis software must be resident in the CAM system. This software correlates the data from different sources, analyzes and characterizes the data, in a reasonable time, so that accept/reject decisions can be made for each wafer. Coordination and correlation of parametric and physical data is mandatory for the institution of this procedure. The foundry must not only demonstrate control of the process, but also control of the data.

In-line quality control procedures must also be used and require that results be entered into the CAM system. Only when the wafer has met all the manufacturer's quality criteria during fabrication can it be submitted for Wafer Acceptance Testing.

2.2.5 Description of Modules

2.2.5.1 Process Control Monitor (PCM). Five PCM chips or Drop-in Test Circuits (DITC) are located on each wafer. Typical locations of these PCMs would be one in each quadrant and one in the center (Figure 1, Pg. 40). The PCM will contain an extensive collection of test structures to enable complete characterization of the process. A table of recommended parameters and typical structures is shown in Table 1 (Pg. 36 - 37). Included in the PCM are the identical structures, electrical parameter category, contained in the Test trip. Also included would be physical parameters, global defect parameters, circuit function and Reliability structures.

2.2.5.2 Test Strips. A test strip is a collection of structures placed in the kerf or scribe lane beside each die on a wafer. The test strip contains all structures required for electrical parameter measurements shown in Table 2 (Pg. 38), connected to probe pads for wafer probing.

2.2.5.3

Reliability Evaluation Module (REM). These structures shall provide an assessment of process stability as a function of time. Ideally, these structures would be designed for accelerated stress testing such that all Reliability tests could be performed on wafer. If this were not possible, the REMs would have to be removed and packaged for testing. The REMs should preferably be located in the same areas as the PCMs. Depending on the structures designed, it could be possible to place the REM inside the PCM with an inner ring of probe pads similar to Figure 2 (Pg. 40). These probe pads could then be bonded if required for tests requiring packaged samples. Suggested Reliability parameters are shown in Table 3 (Pg. 39). It should be noted that there could possibly be an overlap of PCM and REM structures.

2.2.5.4

SEM Cross-section Array. A SEM cross-section array is a collection of structures arranged in a manner to allow a single cross-section to reveal maximum information about a processed wafer. Since all possible structure cross-sections would be revealed, this would permit the characterization of the process in a minimum amount of time. Micro sectioning procedures are well known and can be practiced by all foundries. The array is located on the PCM and can also be placed on the REM or each CM² die, if space permits.

2.2.5.4.1

Application SEM Cross-section Array. Ideally, a SEM cross-section array evaluation should be applied to each wafer, if it is to be consistent with the philosophy of wafer acceptance. This, of course, would be unrealistic, since cross-section analysis is a lengthy process. A more practical approach would be the random selection of a sample PCM, for cross-section evaluation, from the accepted wafers (lot). If the cross-section meets all requirements the lot

is accepted. If the cross-section does not meet the requirements the lot is rejected. However, as an alternative to rejecting the entire lot, the manufacturer may choose to evaluate the cross-section on an individual wafer basis. Using this procedure, a wafer which meets the cross-section requirements would be accepted. Those which did not meet the cross-section requirements, would be rejected.

In addition to the above, a SEM cross-section inspection test method, similar to 2010, must be generated, for each technology. Inspection criteria for each thin film, diffusion, and its profile would have to be written. This would be a very complex specification and probably a larger issue than sample selection criteria.

2.3 Manufacturer and Line Certification Procedures for VLSI/VHSIC Assembly (Appendix A3).

2.3.1 Background. This proposed procedure is intended to supplement existing (MIL-STD-976A) procedures for purposes of certifying VLSI/VHSIC assembly lines. Appendix B of the proposed procedure details specific requirements for certifying large area die attach, wire bonding, assembly cleaning and sealing processes. Appendix C proposes procedures for certification of tape automated bonding (TAB) fabrication processes. Certification procedures are included for the following:

1. Passivation Evaluation and Wafer Preparation
2. Barrier and Field Metal Deposition
3. Photolithography for Bumping
4. Bump Electroplating
5. Inner-lead Bonding
6. Outer Lead Bonding
7. Package Seal

The TAB process certification procedures represent the first attempt to define TAB process controls for military and space hardware, and should provide the basis for discussions between the government and military suppliers involved with TAB processes for both board and hermetic package assemblies.

2.4 Certification Procedures for VLSI Microcircuits Facilities and Lines (Appendix A4).

- 2.4.1 Background. The intent of the proposed procedure is to provide a plan for baseline certification of VLSI/VHSIC manufacturing facilities, in a format similar to MIL-STD-1772. The current procedure (MIL-STD-976A) audit requirements (contained in Paragraph 4.1.2) state: "...the purpose of the audit is to determine that the controls imposed on manufacturing, inspection, and testing of JAN microcircuits are sufficient to assure conformance with the requirements of MIL-M-38510 and this standard". This requirement is not sufficient to insure that the manufacturer can produce high complexity, micron/sub-micron devices with consistent yields. A uniform method is required for evaluating a manufacturers' capabilities to produce parts with the same electrical parameters to a given set of design rules.

We have proposed specific methods in the Vendor Validation Procedure (see Appendix A1, Sections 5,6, and 7) that could be used for the process capability demonstration requirements. It is not intended, nor possible, to impose standard test structures to demonstrate process capability. However, the requirements for the type of physical and electrical parameters to be measured on the test structures, and the measurement methods, should be met by the manufacturer's own test structure(s). Verification of the conformance to these requirements will be part of the pre-survey audit by the certification team.

The use of CAM for data analysis and die/wafer tracking has been proposed as a part of the Wafer Lot Acceptance procedure. The assessment of the vendor's use of CAM has been included, therefore, in the line certification requirements. The sections immediately following provide some guidelines for auditing the CAM capabilities of the supplier.

3. COMPUTER AIDED MANUFACTURING (CAM).

- 3.1 Background. An understanding of the application of CAM equipment and facilities controls to VLSI/VHSIC fabrication is required in order to establish guidelines for government assessment of potential suppliers capabilities. This section describes the principle areas of application. Typical data outputs from ITT Semiconductors CAM systems are in Appendix B.
- 3.2 Data Acquisition and Analysis. Data taken at every measurement/inspection step in the process flow sequence is put into the computer terminal, with wafer lot and individual wafer identity. Computer programs for plotting statistical data (mean value, range, standard deviation, etc.) provide charts for statistical process control (see page 124) and can be used to prevent lot movement if data is out-of-specification (when tied into a wafer tracking system (see 3.3)).
- 3.3 Wafer Tracking System (WTS). This is a computerized system that performs the following functions:
 - 3.3.1 Controls each lot's movements to insure that wafer lots complete each process step in proper sequence. It does this by printing out a step traveller (see page 126) sequentially after each major process step is completed. A step traveller will not be issued unless the previous major step has been completed, and data (if there is a data input requirement) is within specification.
 - 3.3.2 Prints out key process parameters/operator instructions for the particular lot, and process. Typical parameters are: equipment identification and program identification, sampling plan/accept reject limits for tests, flow sequencing for test wafers, mask level identity and revision letter (for photo steps).

- 3.3.3 Controls (limits) photomask usage and issue. The computer tracks and limits the number of times a photomask can be used before cleaning or replacement. For critical alignments, it may be programmed to specify the individual aligner to be used for a particular mask level and/or mask serial number.
- 3.3.4 Verifies equipment maintenance and calibration. This utility compares preventive maintenance and calibration schedules for every production equipment with actual performance dates and prevents a lot from being processed with equipment that requires preventive maintenance or calibration. Another safeguard is provided by equipment status flags that prevent lot processing through equipment in "down" status. (Microprocessor-controlled equipment may have this flag built into the software programs).
- 3.3.5 Reworked lot control. Allowable rework on discrepant lots (or serialized wafers in a lot) is defined as an alternate path in the wafer process sequence. Sublots can be created, rework travellers issued for the rework processing, and lot hold provided for remaining wafers.
- 3.3.6 Tracks status of wafer lots in process. This is a production control function that identifies the number of wafer lots/wafers at each major process step, the total number of wafer moves, the total number of wafers in process (WIP).
- 3.3.7 Provides lot history. Documents complete lot history: starting material, levels and serial numbers of masks used, material review board (MRB) documentation (see Par. 3.6), causes of wafer dropout, rework history, critical dimensions and parametrics summary.

- 3.4 Facilities Controls. A computer is usually dedicated to monitoring and control of facilities required for manufacturing. The intrinsic defect density of the starting wafer material, plus the contributed defects caused by handling, processing and the environment are major determinants of device yield. Continuous facilities controls and monitoring of critical process areas, are essential requirements for successful device manufacture. The types and locations of typical environmental monitors are shown in Table I.

TYPICAL ENVIRONMENT CONTROLS

TABLE I.

<u>LOCATION</u>	<u>TEMPERATURE</u>	<u>HUMIDITY</u>	<u>AIR FLOW</u>	<u>PARTICLE COUNT</u>
Thin Films	X	X	X	X
Photo	X	X	X	X
Furnace		X	X	X
Ion Implant	X	X	X	X
Air Lock			X	X
Gowning Area			X	
Pre-filter			X (1)	
Hepa-B			X (1)	
Etch	X	X	X	X
Probe	X	X		

NOTE (1) - Pressure Drop Monitor.

- 3.5 Gas/Deionized Water Monitoring. In-line sampling of moisture content in gases used in critical processes (except for ion implant) and deionized water parameters can be tied into a control computer for real-time monitoring and alarms for out-of-specification conditions. Water parameters that can be monitored automatically are resistivity, silica content, and particulates.

3.6 Discrepant Material Documentation. Documentation of cause, disposition, and corrective action on non-conforming work-in-process should be part of the CAM system. Computerized sort programs allow supervisors and management to spot equipment, people and processes causing repetitive problems. When tied into the wafer tracking system, discrepant lot movement can be halted for the Material Review and resumed after satisfactory disposition (by controlled access personnel). This system is currently used by ITT Semiconductors (a typical printout of a complete material review action is shown on page 123). The sort programs also aid in yield and failure analysis.

3.7 CAM Equipment. Closed-loop CAM equipment is used in many critical wafer processing steps in VLSI manufacture. In closed loop control systems, the key processing parameters are monitored and electrical signals generated that provide automatic corrections of operating conditions when they exceed pre-programmed limits, or equipment shut-down when the end-point of the process is detected. Examples of CAM equipment with closed-loop process control systems are furnaces for thin film deposition/doping, reactive-ion etching and stripping equipment and metallization systems. Alarms, lockouts to prevent insertion of wafers into equipment that is not within programmed operating limits, are also features incorporated into most state-of-the-art CAM equipment, with or without closed-loop controls.

Process control in closed-loop systems can be critically affected by the accuracy of the sensors that provide the process correction, or termination signals. Maintenance of calibration of these sensors may not be technically feasible when no traceable standards exist, or economically justifiable when downtime of non-redundant equipment cannot be tolerated.

Other techniques to determine when CAM equipment is not providing the required degree of control are essential. The most important is, of course, statistical process control. Proper application of statistical controls to detect non-random causes of process deviations can be used to flag the need for equipment maintenance and calibration.

4. STATISTICAL QUALITY CONTROL (SQC)

- 4.1 Process Control. Precision controls are required on thin films, mask geometries/defects, critical dimensions on both masks and wafers, photolithography and implants to achieve even minimum yields in VLSI/VHSIC wafer processing. Statistical process controls must be maintained on all critical process steps.

There are SQC software packages commercially available to plot and analyze process control charts. Data for plotting may be entered manually, or can be input automatically from the measurement tool or test equipment. The optimum arrangement, however, is to input the SQC data into the CAM system. If wafer tracking system software is designed to process this data, then quick feedback is available on process trends, tooling or equipment problems. Alarms can also be built into the system to warn when data points are outside warning or control limits, or when data patterns indicate corrective actions are required on process and/or equipment.

- 4.2 Indirect Monitoring Applications. Sometimes the measurements made at the conclusion of a process provide an effective means for monitoring the inputs to it. Continuous monitoring of gases used for thin film depositions (e.g. - nitrogen, oxygen used in gate oxidations) requires expensive equipment, that is also costly to maintain and calibrate.

Time-sequential control charts of gate oxide thickness can be more effective indicators of variations in gas moisture content or gas flow rates than the input monitor(s). Another example is the use of wafer mapping of threshold voltage/resistivity to verify uniformity of implant dose/energy patterns across the wafer.

4.3 Process Validation and Yield Enhancement.

- 4.3.1 Mapping of wafer functional test data can identify repetitive zero-yielding sites caused by mask defects.

- 4.3.2 Mean and standard deviation data from process validation module test parameters show process reproducibility from lot-to-lot and from wafer-to-wafer.
- 4.3.3 Analysis of wafer electrical test data from highest and lowest yield wafers in a lot (high-low analysis) is a powerful tool for yield enhancement engineers.
- 4.4 Incoming Wafer Control. Requiring vendors to provide SQC data taken on the batches/lots comprising the shipment can reduce or eliminate duplication of inspection. Acceptance of incoming wafers without sampling inspection could be based on yield history as well as vendors data. This requires that the wafer supplier's identity be maintained on each wafer lot.

5. GUIDELINES FOR ASSESSMENT OF CAM FACILITIES

- 5.1 Baseline Control. The manufacturing baseline defines the manufacturing steps, both major and minor, the critical parameters to be monitored and controlled, (with limits defined), the degree of monitoring required (sampling plans), the process monitors and their degree of monitoring. Typically, a flow chart is used to show the sequential process steps, inspection and measurement points, and process identification numbers. A lot or step traveller provides the operator instructions required for a specific process.

In CAM manufacturing facilities, part or all of the manufacturing baseline is defined in computer software. The control and maintenance of the manufacturing baseline is dependent on the degree of control of the software (and firmware) that defines the manufacturing process. How a manufacturer monitors and controls access to the manufacturing database must therefore be an important part of CAM facilities assessment.

- 5.1.1 Process Specifications, Access and Change Control. CAM system access to change processes, operator instructions, inspection, test parameters and mask tooling, must be defined and controlled. Records of changes, who made them, and authorization for change (process-change authorization number) should be automatically recorded. Access should be restricted to authorized personnel only. Software security must be zealously guarded. Software should have positive means to prevent unauthorized changes (as a minimum, the process-change authorization identity should be required.)
- 5.1.2 CAM Equipment Change Control. Program changes made by keyboard entry are vulnerable to uncontrolled changes. Methods of controlling access to changes and verification of process parameters should be part of the CAM facilities assessment. Program identification should be part of the manufacturing baseline and be automatically printed on the lot traveller.

5.1.3 CAM Configuration Control. The identification of the mask tooling is part of the manufacturing baseline. The revision status of a set of mask tooling should be a unique code that requires modification any time any mask in a set is revised. Baseline manufacturing processes, and their variants, should also be uniquely identified to minimize errors in manufacture. Process modifications to optimize yield for a specific device must be uniquely identified in computerized wafer tracking systems and tied in with the device number on the travellers.

5.2 Facilities Controls

5.2.1 Clean Room Air. Facilities Controls should be part of the CAM system. This will facilitate real-time monitoring (usually by multi-point sampling of critical processing areas) of air temperature, humidity, and particle count. Verification of proper air-flow rates and positive air pressure in the clean-room, air-locks, and gowning areas should be a documented part of the facilities maintenance procedures.

5.2.2 Deionized Water. Water resistivity monitoring should be continuous at the source and should be tied into the computerized facilities monitoring system for alarm and facilities shut-down. Periodic verification of silica content and bacteria count should be part of the plant maintenance procedure. Resistivity monitoring at critical points-of-use should be incorporated in the process procedures.

5.3 Data Entry. Data entry of in-process measurements intended for process control must be protected from unauthorized change. If lot-movement is dependent on computer verification of process parameters, changes in specific limits should be subject to the guidelines in Paragraph 5.1.1.

- 5.4 Discrepant Material Review. Discrepant material disposition should be a part of the CAM system input. Satisfactory disposition by authorized personnel should be required as a system entry before lots can be moved to the next processing step. Computer verification of wafer count (number waived, number scrapped, number reworked) after disposition should be included in lot movement control.
- 5.5 Data Tracking. The CAM system should be capable of maintaining individual wafer identity through the entire wafer manufacturing, test and assembly operation. Ideally, the output of the wafer test (D.C. parametric, functional probe) should also be part of the data tracking system so that any data taken as part of in-process control can be correlated with parametric and functional probe data.

6. CONCLUSIONS AND RECOMMENDATIONS

The existing procedures for microcircuit screening and qualification (Methods 5004, 5005, MIL-STD-883C) are no longer adequate for insuring the reliability and uniformity of VLSI/VHSIC Devices. The rapidly increasing circuit density of those devices makes 100% die visual inspection an ineffective and costly screening procedure. Burn-in screening is still the most effective reliability screen, although it is becoming more and more difficult and costly to define circuitry to effectively stress all the critical device modes. Reliability Evaluation Module (REM) Testing at the wafer level, discussed in this report, will supplement burn-in as a reliability screen. However, extensive studies must be performed to correlate failure rates of VLSI/VHSIC Devices screened by burn-in with REM testing. We have proposed, and recommended, that the REM structures be used as part of the wafer acceptance tests, but leave open their use as substitutes for circuit burn-in or life test.

Inherent in this study of quality procedures was the assumption that as chips approach the complexity of whole systems, the reduced chip volume required could be produced primarily by silicon foundries, either independent or subsidiaries of merchant manufacturers. We recommend the procedures proposed in this report for evaluating and certifying these foundries form the basis for modification of the existing MIL-STD-976A line certification method.

We have also proposed as a replacement for the existing Method 5007 (MIL-STD-883) a wafer acceptance procedure that incorporates reliability screening, process quality evaluation, and electrical parameter testing of each wafer in a lot. Consideration also should be given to use of this procedure as a substitute for some, or all, of the screening requirements of Method 5004, MIL-STD-883. This would require agreement on a Reliability Evaluation Module (or chip) and test insert structures to be inserted in product wafers.

We also recommend that the guidelines for the evaluation of computer-aided-manufacturing (CAM) facilities generated in this study be incorporated into a revised line certification procedure. The use of CAM is an essential requirement for manufacturing control as well as quality assurance. The extensive data tracking and analysis required for the proposed wafer acceptance procedure mandate the use of computerized lot tracking and wafer testing.

APPENDIX A1

VENDOR VALIDATION PROCEDURE

VENDOR VALIDATION PROCEDURE

- 1) Scope
- 2) Technology Assessment
- 3) Process Specifications
- 4) Electrical Specification
- 5) Validation Procedure
- 6) Validation Methodology
- 7) Wafer Foundry Vendor Acceptance Criteria

1.0 SCOPE

- 1.1 Purpose: This standard defines the procedure for selecting a wafer foundry to manufacture VHSIC type MOS custom or semi-custom integrated circuits.

2.0 TECHNOLOGY ASSESSMENT

- 2.1 Purpose: This procedure describes the method for evaluating a vendor's technology compatibility and manufacturing capability.
- 2.2 Design rules: The design rules define the characteristics of the technology and the guidelines for mask layout design. It should contain the following:
 - 2.2.1 Description of the process steps and functions of each mask layer.
 - 2.2.2 Process specifications which define the junction depth, sheet resistivities, intermediate oxide thicknesses and interconnect conductive layer thicknesses.
 - 2.2.3 Electrical parameter specifications which define the essential device design parameters such as threshold voltage, breakdown voltage, transconductance, junction capacitance, body effect, field device threshold voltage, etc.

- 2.2.4 Geometric layout design rules which define physical dimensions and their relationships to neighboring elements.
- 2.2.5 Mask alignment sequence and its allowable tolerances.
- 2.2.6 Mask polarity and sizing requirements.
- 2.2.7 Guidelines relating to packaging and handling.
- 2.3 Maturity: This section defines the method used to assess the maturity of the technology.
 - 2.3.1 Starting date: The date the technology development program started.
 - 2.3.2 Completion date: The date the technology development completed, fully documented and ready to be transferred from development laboratory to production line.
 - 2.3.3 Characterization data: Complete process characterization information will provide the characteristics and quality of the technology.
 - 2.3.4 Technology transfer history: When the technology transfer occurred and completed.
 - 2.3.5 Production history: When was the first product delivered and how many products have been delivered and at what volume.
 - 2.3.6 Production status: How many products using this technology and how many more devices are in design.
 - 2.3.7 Yield history: What is the line yield and net product yield and its corresponding defect density.
 - 2.3.8 Future plan: What is the plan for technology upgrade and yield improvement.
 - 2.3.9 What is the life expectancy of the technology.
- 2.4 Capacity: This section defines the method used to assess the vendor's manufacturing capacity.

- 2.4.1 Line capacity: The throughput of the wafer fabrication line such as the size of the wafer, the output number of wafers per day or per week, etc.
- 2.4.2 Line yield: The number of good wafers versus the number of wafers started.
- 2.4.3 Technologies: How many different type technologies are running through the same fabrication line.
- 2.5 Facility: Utility and facilities required to support volume manufacturing.
 - 2.5.1 Office space: Includes administrative and engineering office, laboratory and library, etc.
 - 2.5.2 Clean room: Area of dust free clean room and its classification.
 - 2.5.3 Equipment: Age and condition of the manufacturing equipment.
 - 2.5.4 Test facility: Type, condition and capacity of the test equipment.
 - 2.5.5 Packaging facility: What type package the vendor's equipment can handle and what is the capacity. Is the equipment automated or semi-automated.
 - 2.5.6 Reliability facility: The burn-in oven, shock test, radiation test, ESD test and SEM equipment and its condition.
 - 2.5.7 Material control facility: Incoming inspection and control of all the materials such as silicon wafers, masks, chemicals, etc. The type of equipment used for inspection and the method used for control and distribution of the materials must be evaluated.
 - 2.5.8 CAM facility: The ability of using computers to assist in manufacturing such as wafer tracking, process control, data acquisition and data analysis.

3.0 PROCESS SPECIFICATION

- 3.1 Purpose: This specification defines the process technology and its characteristics. It will be the most important document used for wafer foundry vendor selection.
- 3.1.1 Starting material: Defines the material type, crystal orientation and its resistivity or concentration.
- 3.1.2 Wafer specification: Defines the thickness, size and flatness.
- 3.1.3 Mask layer: Defines the function of each mask layer and its critical dimension.
- 3.1.4 Alignment: Defines the mask alignment sequence and its tolerance. Visual test patterns are used to determine actual tolerances for a wafer.
- 3.1.5 Intermediate oxide and conductive layer thicknesses: Field oxide, intermediate oxide, passivation oxide, poly and metal thicknesses can all be measured visually by a SEM cross sectional analysis or equivalent means. Field oxide thickness should be measured between minimum spaced active areas as well as in open areas free of active regions. In addition, gate oxide thickness can be obtained by conventional electrical C-V measurements.
- 3.1.6 Junction depth: All diffusion junction depths may be measured by use of a spreading resistance probe test or equivalent. Accuracy of the spreading resistance probe measurement depends critically on the measurement accuracy of the angle of cross section.
- 3.1.7 Junction leakage: Defines the PN junction leakage current under reverse bias condition. This can only be measured using very large junction areas.

- 3.1.8 Diffusion, poly, and metal sheet resistivities: Sheet resistivities for all diffusions (N+, P+, p-well, n-well), poly (first level poly doped N+ or P+, second level poly), and metal layers may be measured using a Van der Pauw cross resistor (Reference: Buehler, M.G., S.D. Grant, and W.R. Thurber, "Bridge and van der Pauw Sheet Resistors for Characterizing the Linewidth of Conducting Layers," J. Electrochem. Soc., 125 (4), 650-654 (April 1978).) or equivalent structure. Care must be taken to ensure that the current density does not create abnormal thermal stresses.
- 3.1.9 Contact resistance: A Kelvin contact resistance structure should exist for each possible contact type allowed by the design rules (typically metal to metal, metal to poly, or metal to diffusion). Care must be taken not to exceed the current density specification of the contact geometry.
- 3.1.10 Line/space measurement: Each layer should contain patterns which can be measured by a SEM cross sectional analysis or equivalent means to ascertain if all critical dimension specifications are met. Alternatively, for conductive layers, a well defined Kelvin resistor geometry in conjunction with an accurate sheet resistivity can be used to calculate the line width and spacing. A split-cross bridge pattern can be used for this purpose.

All metal and poly layers should also contain structures reflecting the minimum pitch allowed in the design rules. These pitch tests should contain worst case steps and topological conditions. The integrity of each line should be verified and the absence of shorts between adjacent lines checked. This may be done electrically or visually.

4.0 ELECTRICAL SPECIFICATION

- 4.1 Purpose: This specification will define the electric parameters which will be used by the design engineer for chip design and also will be used as a measurement of wafer acceptance criteria.
- 4.1.1 The following list contains electrical parameters which should be included. For each parameter, typical test conditions are given. All parameters tested

should be performed on minimum geometry devices unless specified differently by the design rules. Test temperature condition for all parameters is room temperature (25° C) ambient.

<u>Electrical Parameter</u>	<u>Test Conditions</u>	<u>Procedure</u>
Threshold Voltage (V_{T0})	$V_{GS} = V_{DS}$ $V_{SB} = 0$ volts $V_{T0} = V_{GS}$ at $I_{DS} = 0$ A	A series of V_{GS} measurements are made for various I_{DS} values. Using the equation $I_{DS} = (K'W/L)(V_{GS}-V_{T0})^2$, V_{T0} is extrapolated as being V_{GS} for $I_{DS} = 0$ A.
Body Effect (γ)	$V_{GS} = V_{DS}$ $V_{SB} = 0$ volts $V_T(V_{SB})$ defined as V_{T0} above, except V_{SB} is not constrained to 0 volts. Φ = strong inversion = .6 to .65 volts.	A series of $V_T(V_{SB})$ measurements are made for various V_{SB} values. Using the equation: $V_T(V_{SB}) = V_{T0}(V_{SB} = 0) + (\sqrt{V_{SB} + \Phi} - \sqrt{\Phi})$ The body effect, γ , is found from the slope of the plotted values.
Punch Through Breakdown Voltage (V_{BPT})	$V_{GS} = V_{BS} = 0$ volts V_{DS} is varied.	The punch through breakdown voltage is defined as that drain voltage which causes $I_{DS} = 10 \mu A$ to flow.
Junction Breakdown Voltage (BV_{PN})	p side of junction is biased negative with respect to the n side of junction.	The junction breakdown voltage is defined as that reverse biased junction voltage which causes $10 \mu A$ to flow across the junction.

<u>Electrical Parameter</u>	<u>Test Conditions</u>	<u>Procedure</u>
Field Threshold Voltage (V_{TF})	$V_{SD} = V_{DD}$ $V_{SB} = 0$ volts V_{GS} is varied	The field threshold voltage is defined as that V_{GS} value which causes $I_{DS} = 1$ A to flow. An alternative approach is to force $V_{GS} = V_{DS}$ and $V_{SB} = 0$ volts. Then, V_{TF} is defined as the V_{GS} value which results in $I_{DS} = 1$ A to flow. This alternative approach measures the lowest of punch through breakdown, junction breakdown, or field threshold.
Transconductance (g_m)	$V_{GS} = V_{DS}$ (to be specified) $V_{SB} = 0$ volts	The transconductance in saturation is found using the equation $g_m = 2\sqrt{(W/L)K' I_{DS}}$ wherein a fixed specified V_{DS} value determines the bias point of the device.
Effective channel length and width (L_{EFF} , W_{EFF})	$V_{DS} = 0.1$ volts $V_{GS} \gg V_T$ $V_{SB} = 0$ volts	To measure effective channel length, the channel conductance (I_D/V_D) is measured for a set of gate voltages in the linear region for two or more transistors of the same width but with different lengths. The channel resistances are plotted against the drawn channel length. The projection of the intersection point of these lines on the channel length axis is the $\Delta L = L_{drawn} - L_{eff}$. Effective channel width can be determined the same way using transistors of the same length but varying width.

5.0 VALIDATION PROCEDURE

- 5.1 Purpose: This procedure defines the methodology used to verify the vendor's process against a set of process and electrical specifications.
- 5.2 Historical data: The easiest and most economical way to validate a vendor's process is to use the existing historical data. The necessary data should include the process characterization report, yield data, and reliability data.
- 5.3 Process Control Monitor Data: If the technology is new or there is no historical data available, then the vendor's in-line process control monitor data can be used for validation purposes provided that all the essential process and electrical parameters can be measured from this monitor. The disadvantage of this method is the lack of quantitative and statistical data.
- 5.4 Specific Process Validation Module (PVM): A specially designed process validation module which contains all the test structures to verify process and electrical parameters. A Reliability Evaluation Module (REM) acceptable to the procuring activity must be incorporated in the test structures as part of the certification process. This PVM should have the following characteristics:
 - 5.4.1 All essential process and electrical parameters must be testable.
 - 5.4.2 Ease and speed of testing must be emphasized for automated test environment.
 - 5.4.3 CAM capability for data analysis and tracking must be available.
 - 5.4.4 Test devices must be accessible for assembly.
 - 5.4.5 All test data including packaged devices must maintain the wafer number and lot traceability.

- 5.4.6 A commonly used electrical and process parameter measuring method is defined previously in Sections 3 and 4.

6.0 VALIDATION METHODOLOGY

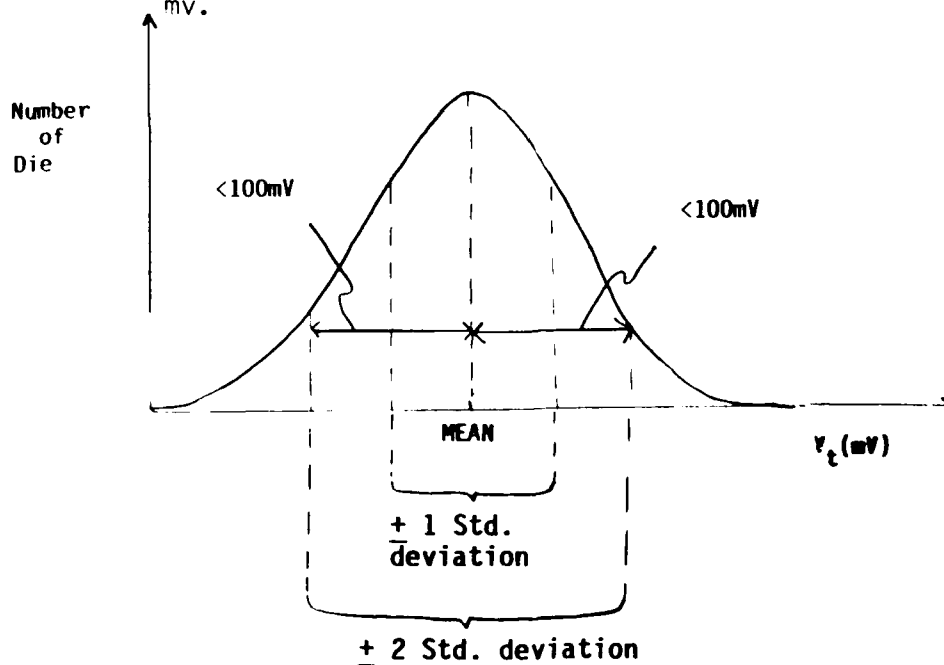
- 6.1 Purpose: This section defines the method for using a specific PVM to validate a vendor's process. The procedures defined in Sections 5.2 and 5.3 are, in effect, comparing a collection of data against a set of specifications which is very similar to this section.
- 6.2 Validation methods:
 - 6.2.1 Design or select a specific PVM.
 - 6.2.2 Generate a dedicated mask set which contains only the specific PVM.
 - 6.2.3 Fabricate three lots of wafers at two to four week intervals. Each lot should have a minimum of 10 wafer starts.
 - 6.2.4 Test all wafers and collect the data. All data must maintain the traceability to die location.
 - 6.2.5 Assemble a minimum of 40 devices from each lot and maintain the traceability.
 - 6.2.6 Perform temperature and stress test per process and electrical specifications.
 - 6.2.7 Collect the temperature drift data.
 - 6.2.8 Perform ESD and other reliability test per the reliability requirements defined in the Wafer Lot Acceptance Procedure.
 - 6.2.9 Conduct data and failure analysis.
 - 6.2.10 Summarize results and compare with the process and electrical specifications.

7.0 WAFER FOUNDRY VENDOR ACCEPTANCE CRITERIA:

7.1 Purpose: This section defines the criteria used to select or reject a wafer foundry vendor. While analyzing the test data, some of the extreme data should be statistically eliminated to minimize the error on mean value and standard deviation calculations.

7.2 Acceptance Criteria:

- 7.2.1 All parameters mean value (plus or minus two standard deviations) must be within the specified range.
- 7.2.2 All wafers must have at least 70 percent of the tested devices meet the process and electrical specifications.
- 7.2.3 Each wafer lot must have a minimum of 70 percent line yield.
- 7.2.4 Two standard deviations of threshold voltage (see example below) on the same wafer must be less than 100 mv.



- 7.2.5 Two standard deviations of threshold voltage (see example above) between wafers must be less than 250 mv.
- 7.2.6 The threshold voltage drift after stress must be less than 200 mv.

APPENDIX A2

PROPOSED WAFER ACCEPTANCE PROCEDURE

PROPOSED WAFER ACCEPTANCE PROCEDURE

1.0 SCOPE

Wafer Acceptance Testing shall be performed on all approved wafers (met all quality criteria during fabrication) from each lot.

2.0 WAFER EVALUATION REQUIREMENTS

There are five phases to Wafer Acceptance:

1. Process Control Monitor (PCM) or Drop-in circuit Test
2. Test Strip Test (in Kerf)
3. Complex Monolithic Microcircuit (CM²) Test
4. Reliability Evaluation Monitor (REM) Test
5. SEM Cross-section Array Evaluation

Refer to Flow Charts Figure 3a and 3b.

Note: The following procedure will assume packaged REM evaluation Figure 3a.

2.1 PCM Evaluation

Each PCM die on a wafer shall have parameters, listed in Table 1, tested to the applicable specification. Electrical test parameters, values, limits (including deltas) and conditions, shall be specified in this specification.

2.1.1 PCM Pass/Fail Criteria

A wafer is considered as Passing PCM Tests, if all PCM parameters listed in Table 1 have met the specification in all five (5) PCM locations on the wafer. This wafer may then proceed to CM² test (2.3).

A wafer is considered as failed and rejected if any one parameter fails at all PCM locations on the wafer. No further tests would be performed on this wafer. This failure is defined as a "killer defect".

If a wafer fails one or more parameters on a PCM, but on a combination of all 5 PCM's passes all parameters, the manufacturer, as an alternative to rejecting the wafer, may elect to use the test strip evaluation procedure (2.2).

2.2 Test Strip Evaluation

A wafer submitted to this test must have all test strip parameters listed in Table 2 tested to the applicable specification. Electrical test parameters values, limits (including deltas) and conditions, shall be specified in this specification.

2.2.1 Test Strip Pass/Fail Criteria

A wafer is considered as passing Test Strip tests if 25% or more of the test strips pass all parameters. This wafer shall be mapped with all CM² die adjacent to the passing test strips identified as candidates for CM² test. Since there are test strips on both sides of the CM² die, both test strips must pass all parameters for the CM² die to be a candidate for electrical testing. The remaining die adjacent to failed test strips shall be identified as not acceptable as CM² die and are not required to be tested.

A wafer is considered as failed and rejected if less than 25% of the test strips pass all parameters. No further tests will be performed on this wafer.

2.3 CM² Test

CM² die shall be tested to the applicable specification. Electrical test parameters, values, limits (including deltas) and conditions shall be specified in the specification. All CM² die shall be tested on a wafer which passed PCM test criteria (2.1.1). A wafer which passed test strip criteria (2.2.1) shall have only the CM² die identified for CM² test, tested.

All die which pass CM² test shall be identified as available die for packaging.

This wafer can now be diced with all identified good die placed in storage until Reliability evaluation is completed.

2.4 REM Evaluation

The five (5) REM die from a wafer shall be packaged to the applicable specification. Each REM die shall have the parameters, listed in Table 3, tested to the applicable specification. Electrical test parameter values, limits (including deltas) and conditions shall be specified in this specification.

2.4.1 REM Pass/Fail Criteria

A REM is considered as passed if all REM parameters have met the applicable specification. A REM is considered failed if any parameter does not meet the applicable specification.

2.5 Wafer Accept/Reject Criteria

A wafer which had all five (5) REM die pass the REM criteria (2.4.1), shall be considered acceptable. A wafer which had any REM die fail the REM criteria (2.4.1) shall be considered rejected. All passed CM² die in storage, associated with this wafer are considered rejected and cannot be packaged.

2.6 SEM Cross-section Array Evaluation

A single PCM die shall be selected at random from the accepted wafers which remain from the Lot after all have completed the wafer evaluation requirements. This PCM will be cross-sectioned through its cross section array. The cross-section will be evaluated to the applicable specification.

2.6.1 SEM Cross-section Array Pass/Fail Criteria

A Lot of accepted wafers from which a sample PCM has met all cross-section requirements is considered acceptable. All passed CM² die in storage associated with these wafers are considered acceptable and can be packaged.

A Lot of accepted wafers from which a sample PCM has failed to meet the cross section requirements shall be considered rejected. All passed CM² die in storage associated with this wafer are considered rejected and cannot be packaged.

2.6.2

As an alternative to rejecting all wafers in a Lot which had its sample PCM fail the cross section requirements, the manufacturer may elect to evaluate a single PCM from each of the accepted wafers from the rejected Lot. In this case a single PCM cross-section evaluation will be applied to each wafer. A wafer, from which the sample PCM has met all cross-section requirements is considered acceptable. All passed CM^2 die in storage, associated with that wafer are considered acceptable and can be packaged.

A wafer from which the sample PCM cross-section has failed shall be considered rejected. ALL passed CM^2 die in storage associated with this wafer are considered rejected and cannot be packaged.

TABLE 1

PCM STRUCTURES

<u>Class</u>	<u>Typical Structure</u>
1. <u>Physical Parameter</u>	
Line width	Line-width, space, pitch ¹
Visual or Electrical Alignment	
* Design Rules	Assorted structures
* Etching	Visual Structures
2. <u>Electrical Parameter</u>	
Capacitance	Gate Oxide Capacitor(s)
Contact resistance (small number)	Assorted contact chains
Oxide Breakdown	Gate Oxide capacitor(s)
Resistance	Assorted Van der Pauws
Transistor parameters	Assorted Geometries P & N
* Diode Parameters	Assorted diodes
* Leakage	Assorted transistors
1. Can be measured optically (high magnification) or SEM measurement.	

*Optional

TABLE 1

Continued.

<u>Class</u>	<u>Typical Structure</u>
3. <u>Global Defects</u> (Electrical Parameters)	
Capacitance	Gate Oxide Capacitors
Oxide Breakdown	Large area capacitors
Oxide Integrity	Capacitor Arrays
Contact Resistance	Assorted contact chains (large number of contacts)
Continuity/Bridging	Assorted serpentine structures over steps
Leakage	Transistor Array (large qty.)
4. <u>Circuit Function</u> <i>Circuit function</i>	<i>Ring oscillators, RAMs, F/F etc.</i>
5. <u>Reliability (CMOS)</u> Latch-up	Latch-up structures

TABLE 2

TEST STRIP STRUCTURES

<u>Parameter</u>	<u>Typical Structures</u>
Capacitance	Gate Oxide Capacitor(s)
Contact resistance	Assorted contact chains (small number)
Oxide Breakdown	Gate Oxide Capacitor(s)
Resistance	Assorted Van der Pauws
Transistor Parameters	Assorted Geometries of both P & N type
* Diode Parameters	Assorted diodes
* Leakage	Assorted transistors
* Optional.	

TABLE 3

RELIABILITY EVALUATION MODULE SUGGESTED PARAMETERS

<u>Parameters</u>	<u>Structures</u>
Time dependent dielectric breakdown	TBD
Ionic drift	TBD
Hot Carriers	TBD
Electromigration	TBD
Leakage	TBD
Transistor Parameter Stability	TBD
Contact Resistance Stability	TBD

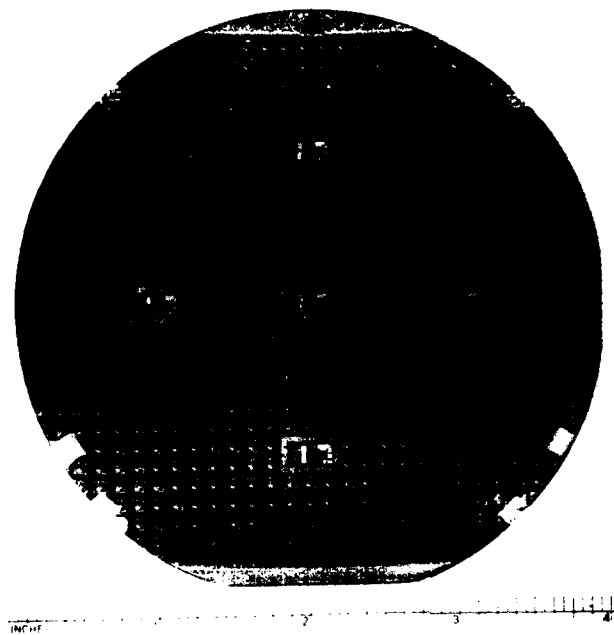


FIGURE 1 - Wafer with Five PCM Locations

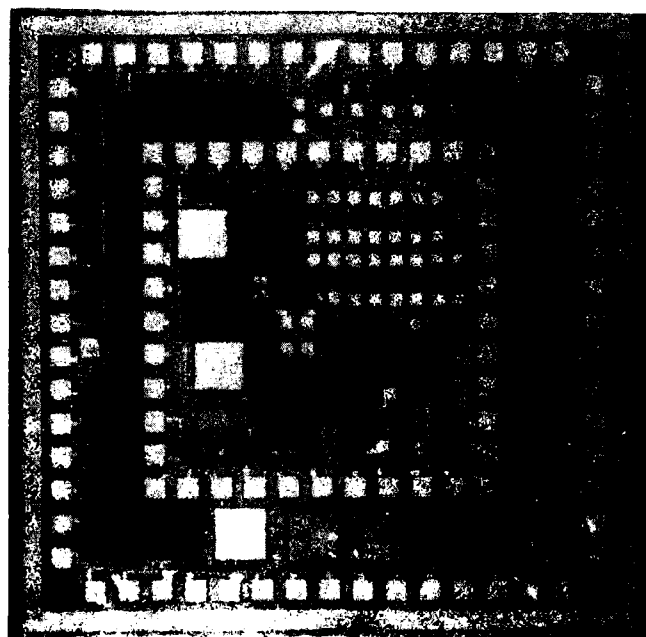


FIGURE 2 - PCM Die Photo Showing Inner and Outer Rings

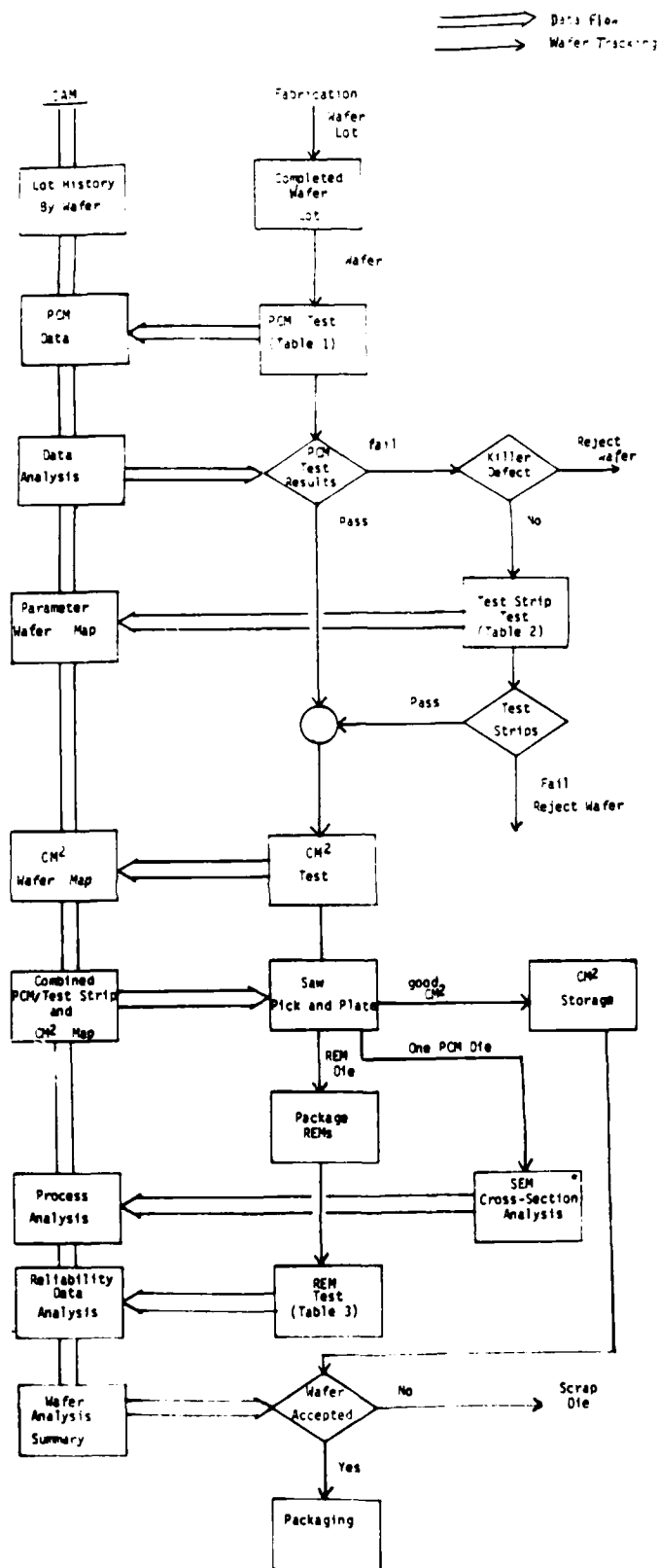


Figure 3a Flow Chart, Wafer Acceptance Procedure using packaged REM evaluation.
 *See Section 5.5

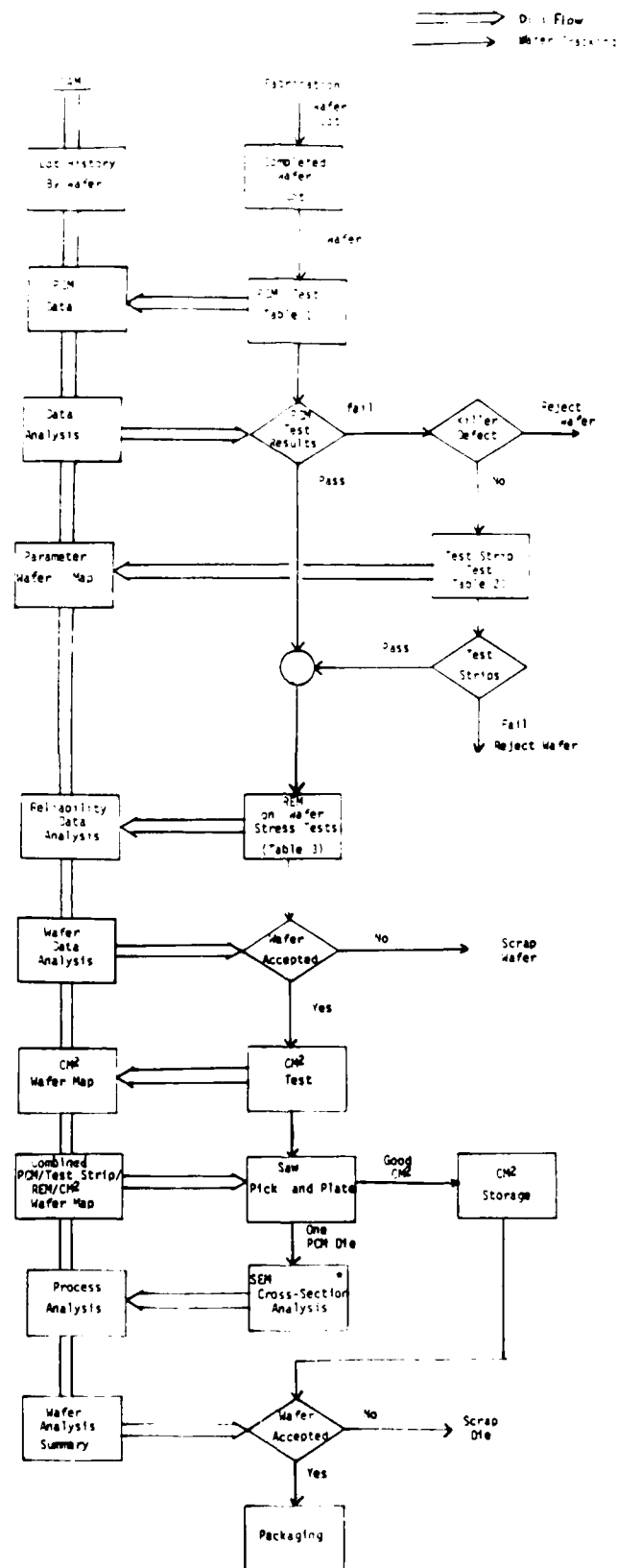


Figure 3b
Flow Chart, Wafer Acceptance Procedure with on Wafer REM evaluation.

*See Section 5.5

APPENDIX A3

MANUFACTURER AND LINE CERTIFICATION

PROCEDURES FOR VLSI/VHSIC ASSEMBLY

MIL-STD

PRODUCT ASSURANCE
PROVISIONS FOR
VLSI/VHSIC MICROCIRCUITS

MANUFACTURER AND
LINE CERTIFICATION PROCEDURES
FOR
VLSI/VHSIC ASSEMBLY

PREPARED FOR:
ROME AIR DEVELOPMENT CENTER
GRIFFISS AIR FORCE BASE, NEW YORK

CONTENTS

1. Scope
2. Referenced Documents
3. Definitions
4. General Requirements
5. Detailed Requirements

APPENDIX A. Audit Plan for Manufacturer and Line Certification.

APPENDIX B. Certification of Die Attach and Wire Bond Assembly Processes.

APPENDIX C. Certification of Tape Automated Bonding Fabrication and Assembly Processes.

1. SCOPE

- 1.1 Purpose. This document establishes minimum requirements governing certification of assembly fabrication processes/line(s) for VLSI/VHSIC microcircuits. It is intended to standardize the documentation and testing procedures for VLSI/VHSIC microcircuits for use in military and aerospace applications. It covers the interface between user and manufacturer and it is not intended to be a complete set of documentation required to build VLSI/VHSIC microcircuits.
- 1.2 Classification. VLSI/VHSIC microcircuits covered by this document include all package sizes, Class B and Class S devices.
- 1.3 Areas of Concern:
- A. All processes are documented.
 - B. All processes under control.
 - C. Conformance to this document and MIL-M-38510.
 - D. Supplier control - procurement documents for parts and materials.

2. REFERENCED DOCUMENTS

- 2.1 The following documents in effect on the date of request for quotation form a part of this standard to the extent specified herein:

SPECIFICATIONS

Military

MIL-M-38510 Microcircuits, General Specification for

STANDARD

Military

MIL-STD-883 Test Methods and Procedures for Microelectronics.

Qualification Process. This section is not intended to direct or select the use of any particular fabrication or handling process. It provides a minimum standardization method of certification to insure that the processes will generate VLSI/VHSIC microcircuits that will consistently meet the requirements of MIL-M-38510.

Exceptions. Due to unusual designs and/or material, exceptions or deletions may be granted and documented in the procuring activity Purchase Order and/or Statement of Work.

Analysis of Results. The detailed qualification plan and specifications must be available for review by the certifying activity representative.

Corrective action or justification is required whenever a condition less than full compliance exists and must be approved by the certifying activity.

Frequency of Testing. Any significant change in baseline specification or document requires approval by the certifying activity -- the certifying activity may chose to:

- Approve the change without further testing
- Require specific testing, or
- Require complete requalification.

3. DEFINITIONS

3.1 Terms and Definitions. The definitions of terms used here shall be as specified in the documents referenced in 2.1.0 and herein.

3.1.1 Certifying Activity. To be determined.

3.1.2 Procurement Documentation. To be determined.

4. GENERAL REQUIREMENTS

- 4.1 Certification Requirements. The following requirements are applicable for the general line certification.
- 4.1.1 Documentation. The manufacturer shall have available for on-site review by the certifying activity documentation that demonstrates process control and test capability as defined in MIL-M-38510.
- 4.1.2 Quality Assurance Verification. Quality Assurance Verification shall be in accordance with MIL-M-38510 Appendix A.
- 4.1.3 Audit. The certifying activity reserves the right to audit the facility in accordance with Appendix A of this document and MIL-M-38510. The Audit Plan of Appendix A herein shall be used for keeping the line certification current.
- 4.2 Qualification of Fabrication Processes. The requirements of Appendix B herein are applicable for certifying and maintaining fabrication processes used in the production of VLSI/VHSIC microcircuits.

5. DETAILED REQUIREMENTS

- 5.1 Audit Plan Per Appendix A. The purpose of the audit plan is to provide a systematic method for determining a manufacturer's conformance to the Product Assurance requirements of MIL-M-38510 and MIL-STD-883. The plan contains audit requirements that serve as the basis for initial and continuing certification for manufacturers of VLSI/VHSIC microcircuits.
- 5.1.1 Method. This procedure details the methods for audit.
- 5.1.1.1 Analysis of Results. The representative of the certifying activity shall provide an exit debriefing immediately following the audit and a summary report, within 30 days, to the manufacturer's quality management. The written summary report shall include specific details of any condition less than full compliance.

- 5.1.1.2 Corrective Action. Corrective action or justification is required whenever any condition less than full compliance exists.

The certifying activity shall review and approve the corrective action.

- 5.1.1.3 Frequency of Auditing. Audits shall be performed annually.

- 5.1.1.3.1. Any change to an approved process shall be in accordance with requirements of MIL-M-38510.

- 5.1.2 Responsibility. The certifying activity shall be responsible for scheduling and conducting the audit, and for reporting the results.

- 5.1.3 Manufacturing Processes. This document is not intended to direct or select the use of any particular manufacturing processes but only to standardize on the minimum auditing required to assure that the processes will continue to generate satisfactory products.

- 5.2 Qualification of Fabrication Processes per Appendix B.
The purpose of this section is to document a systematic and uniform method of qualifying various manufacturers processes. This section provides the methods to establish a baseline and evaluate proposal changes in process, materials or design to assure that such changes will maintain or enhance the quality/reliability of the VLSI/VHSIC microcircuits.

- 5.2.1 Qualified Process. This section is not intended to direct or select the use of any particular fabrication or handling process but provides a minimum standardized method of qualification to assure that the processes will generate VLSI/VHSIC microcircuits that will consistently meet the requirements of MIL-M-38510.

- 5.2.2 Exceptions. Due to unusual designs and/or material, exceptions or deletions may be granted and documented by the procuring activity in the purchase order, and/or Statement of Work.

- 5.2.3 Analysis of Results. The detailed qualification plan and results must be available for review by the certifying activity representative.
- 5.2.3.1 Corrective action or justification is required whenever any condition less than full compliance exists and must be approved by the certifying activity.
- 5.2.4 Frequency of Testing. Any significant change in a certified process or document requires approval by the certifying activity. The activity may choose to:
- A. Approve the change without further testing
 - B. Require specific testing, or
 - C. Require complete requalification.

APPENDIX A
TABLE OF CONTENTS

<u>AUDIT ELEMENT NUMBER</u>	<u>TITLE</u>
1	Supplier Material Control
2	Cleanliness and Atmospheric Control in Work Areas
3	Large Area Die Attach
4	Wire Bond
5	TAB Circuits Attached to Substrate
6	Internal Visual Inspection
7	Package Seal
8	Acceptance of Shipment
9	Design Documentation
10	Workmanship
11	Training
12	Process Documentation
13	Handling and Storage
14	Organic Compounds
15	Failure Analysis

APPENDIX A

AUDIT
ELEMENT NUMBER

TITLE

1

SUPPLIER MATERIAL CONTROL

Requirement: Inspection operations shall be documented as to type of inspection, sampling and test procedures, acceptance-rejection criteria, and frequency of use.

References: MIL-STD-883,
Test Procedures
MIL-M-38510 Appendix A
Inspection of Incoming Materials

DETAILS: Verify conformance to the following as applicable:

APPROVAL N/A COMMENT

Chip:

- A. Chip topology conforms to that specified on manufacturer's procurement document
- B. Incoming visual inspection
- C. Incoming electrical testing
- D. Storage in controlled environment

Package:

- A. Package type conforms to type specified on manufacturer's procurement document
- B. Compliance with MIL-M-38510

Other:

- A. Incoming parts and materials are inspected
- B. Documented procedure for incoming inspection to include: Sampling procedures lot accept and reject criteria, and frequency of testing
- C. Documented procedure for handling discrepant parts and materials

APPENDIX A

AUDIT
ELEMENT NUMBER

TITLE

1

SUPPLIER MATERIAL CONTROL (Cont.)

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

2

CLEANLINESS AND ATMOSPHERIC CONTROL IN WORK AREAS

Requirement: Cleanliness and atmosphere control shall have documented requirements for each area in which unsealed units and component parts are stored, processed or assembled.

References: MIL-M-38510 Appendix A, Cleanliness and Atmosphere Control in Work Areas.

DETAILS: Verify conformance to the following as applicable:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. Specified facility cleaning	_____		
B. Particle count	_____		
C. Temperature and humidity	_____		
D. General housekeeping	_____		
E. Documentation	_____		

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

3

LARGE AREA DIE ATTACH

Requirement: The documentation and performance of the process steps by which large area die are attached to a package shall be evaluated.

References: Method 2019, MIL-STD-883, MIL-M-38510

DETAILS: Verify conformance of the following as applicable:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. In accordance with layout	_____		
Process Controls			
A. Conformance to documentation	_____		
B. Applicable revision	_____		
Organic adhesives for attachments:			
A. Shelf life control	_____		
B. Process conforms to documentation in terms of time, temperature, and effectiveness	_____		
Eutectic material attachment:			
A. Material is in accordance with documentation	_____		
B. Process conforms to documentations in terms of time, temperature, and effectiveness	_____		

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

3

LARGE AREA DIE ATTACH (Cont.)

Company Audited

Performed by

Date

Comments:

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

4

WIRE BOND

Requirement: Wire bonding documentation and operations shall be evaluated to ascertain adequate process control.

References: Methods 2011, 2023, MIL-STD-883, MIL-M-38510

DETAILS: Verify the conformance to the following where applicable:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. For each bonding station			
1. Operating records to indicate conformance to bond strength requirements			
2. Certification			
3. Control settings:			
a. Time			
b. Temperature			
c. Force			
d. Power			
4. Documentation for process operation			
5. Visual aids			
B. For the pull test equipment			
Calibration Procedure:			
1. Frequency of calibration			
C. Corective Action:			
1. Implementation of corrective action			
2. Control of corrective action			

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

4

WIRE BOND (Cont.)

Company Audited

Performed by

Date

Comments:

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

5

TAB CIRCUITS ATTACHED TO SUBSTRATE

Requirement: The documentation and performance of the process steps by which circuit mounted on tape are incorporated into a package shall be evaluated.

References: Methods 2017, 2019, MIL-STD-883, MIL-M-38510

DETAILS: Verify conformance of the following as applicable:

APPROVAL N/A COMMENT

- A. In accordance with layout
- B. In accordance with Method 2017

Process Controls

- A. Conformance to documentation
- B. Applicable revision

Organic adhesives for attachments:

- A. Shelf life control
- B. Process conforms to documentation in terms of time, temperature, and effectiveness

Eutectic material attachment:

- A. Material is in accordance with documentation
- B. Process conforms to documentations in terms of time, temperature, and effectiveness

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

5

TAB CIRCUITS ATTACHED TO SUBSTRATE (Cont.)

Company Audited

Performed by

Date

Comments:

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

6

INTERNAL VISUAL: INSPECTION PROCEDURES

Requirement: Internal visual inspection procedures shall be evaluated for conformance to Method 2017.

References: Method 2017, MIL-STD-883, MIL-M-38510

DETAILS: Verify the conformance to the following where applicable:

	<u>APPROVAL</u>	<u>NA</u>	<u>COMMENT</u>
A. Method 2017	_____		
B. Proper inspection equipment	_____		
C. Workmanship standards	_____		
D. Visual aids	_____		
E. Rejections are documented	_____		
F. Provisions of re-inspecting rework	_____		
G. Contamination control documentation - during handling, transportation, and storage	_____		
H. Damage prevention documentation	_____		

Confirm

A. Monitors rework history	_____
B. Initiates corrective action	_____
C. Monitors corrective action	_____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

6

INTERNAL VISUAL: INSPECTION PROCEDURES (Cont.)

Company Audited

Performed by

Date

Comments:

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

7

PACKAGE SEAL

Requirement: Sealing documentation and operations shall be
evaluated to ascertain adequate process control.

References: Methods 1013, 1018, 2024, MIL-STD-883, MIL-M-38510

DETAILS: Verify the conformance to manufacturing process
documentation:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. Preseal Bake Cycle:			
1. Time	_____		
2. Temperature	_____		
3. Atmosphere	_____		
B. Sealing:			
1. Process documentation in work area	_____		
2. Sealing schedules are recorded and maintained	_____		
3. Atmosphere	_____		
4. Moisture content of atmosphere	_____		
5. Moisture content of packages	_____		

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

8

ACCEPTANCE FOR SHIPMENT

Requirement: The traveler record shall be evaluated for completeness and the units shall be examined for external package requirements.

References: Method 2009, MIL-STD-833, MIL-M-38510

DETAILS: Verify the conformance to the following where applicable:

APPROVAL N/A COMMENT

Review records for following:

- A. Maximum allowed rework
- B. Re-inspection of rework
- C. Evidence of inspection
- D. PDA review

Verify conformance to Method 2009.

Review microcircuit marking:

- A. Legibility
- B. Serialization

Verify special customer requirements.

Company Audited

Performed by

Date

Comments

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

9

DESIGN DOCUMENTATION

Requirement: The manufacturer shall establish a documentation baseline in accordance with MIL-M-38510.

References: Verify that the manufacturer has:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. A Change Control System	_____		
B. The change Control System is implemented and enforced.	_____		
C. Established baseline listing of documents for program(s). As a minimum the documents included the baseline listing as indicated in MIL-M-38510.	_____		
D. Utilizes the applicable revision of the documents pertaining to the approved baseline.	_____		

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

10

WORKMANSHIP

Requirement: The manufacturer's documents shall be in accordance with MIL-M-38510.

References: MIL-M-38510.

DETAILS: Verify existence of the procedures and conformance to the process:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. Rework and repair			
1. Temperature controls	_____		
2. Package rework limitations	_____		
3. Provision for complete rescreening	_____		
4. Element replacement limitations	_____		
B. Wire-Rebonding			
1. Limitations documented for circuit	_____		

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

11

TRAINING

Requirement: The training program and documentation shall meet the referenced document.

References: MIL-M-38510, Appendix A.

DETAILS: Verify conformance to training in the critical VLSI/VHSIC manufacturing processes as applicable:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. Cleaning	_____		
B. Die Attachment	_____		
1. Eutectic for Wire Bond	_____		
2. Inner Lead for TAB	_____		
C. Bonding	_____		
1. Wire Bonding	_____		
2. Outer Lead Bonding for TAB	_____		
D. Rework/Repair	_____		
E. Sealing	_____		
F. Electrostatic Discharge(ESD) Practices	_____		
G. Equipment Setup	_____		

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

12

PROCESS DOCUMENTATION

Requirement: The manufacturing process documentation is used to control and monitor the fabrication processes.

References: MIL-M-38510, Appendix A
Manufacturers' Flow Charts
Manufacturers' Process Specs

DETAILS: Verify conformance to the following as applicable:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. Flow charts detailing receipt of material through shipment	_____		
B. Handling of customer returns	_____		
C. Inspection points	_____		
D. Screening	_____		
E. Rework/Repair cycles	_____		
F. Traveler/Routing card	_____		

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

13

HANDLING AND STORAGE

Requirement: The handling and storage of materials from component parts through the completed and sealed package.

References: MIL-M-38510, Appendix A,
MIL-STD-883.

DETAILS: Verify conformance to the following as applicable:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. Documentation utilized to identify critical handling and storage requirements			
B. Electrostatic Discharge (ESD) Practices followed			
C. Packaging/Protection			
D. Environmental/Atmospheric			

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

14

ORGANIC COMPOUNDS

Requirement: All organic compounds have their own unique requirements for handling, storage and application/usage.

References: MIL-M-38510, Appendix A
MIL-A-87172

DETAILS: Verify conformance to the following as applicable:

	<u>APPROVAL</u>	<u>N/A</u>	<u>COMMENT</u>
A. Materials properly qualified	_____	_____	_____
B. Storage	_____	_____	_____
C. Shelf Life identified	_____	_____	_____
D. Cure conditions identified	_____	_____	_____

Company Audited _____

Performed by _____

Date _____

Comments: _____

APPENDIX A

AUDIT
ELEMENT
NUMBER

TITLE

15

FAILURE ANALYSIS

Requirement: To have the capability of analyzing problems on
VLSI/VHSIC microcircuit so that corrective action can
be effected.

References: MIL-M-38510, Appendix A,
Method 5003, MIL-STD-883,

DETAILS: Verify conformance to the following as applicable:

APPROVAL N/A COMMENT

A. Manufacturer has minimum capability to
perform analysis to test conditions
of Method 5003

B. Manufacturer understands physics of
such failure mechanisms as:

1. Mobile charges
2. Moisture
3. Element mounting materials
(organic/eutectic)

C. Semiconductor Glassivation

D. Electrical Overstress

E. Bonding

Company Audited

Performed by

Date

Comments:

APPENDIX B

CERTIFICATION OF ASSEMBLY PROCESSES

<u>PROCEDURE NUMBER</u>	<u>CONTENT</u>
1	Large Area Die Attach
2	Wire Bonding
3	Cleaning
4	Sealing

APPENDIX B

PROCEDURE NO. 1

LARGE AREA DIE ATTACH

1. PURPOSE

The purpose of this test method is to provide a uniform procedure for evaluating die attachment for VLSI/VHSIC microcircuits and to assure that the process being evaluated will result in satisfactory mechanical strength, adequate heat transfer, and electrical performance properties throughout the life of the VLSI/VHSIC microcircuit. It is also designed to evaluate secondary problems that could arise elsewhere in the VLSI/VHSIC microcircuit. This would include such items as wirebonds (both original bonds and bonds made during the rework cycles) and surface contamination of sensitive devices in the VLSI/VHSIC microcircuit.

2. REFERENCED DOCUMENTS

The documentation required for review at the time of evaluation should include the following items as a minimum:

2.1 Materials

- A. Specification control drawings for all materials
- B. Required incoming inspection
- C. Proper storage conditions

2.2 Processes

- A. Specifications to control critical parameters
- B. Minimum environmental conditions to assure consistent product

3. GENERAL REQUIREMENTS

3.1 Mechanical

- A. Adhesive strength of the element bond to the substrate

- B. For metallic attachment material: long term crystallization effects
- C. For organic attachment material:
 - 1. Entrapped moisture both on the surface and deep within the material. This deep moisture causes volumetric shifts over a time period which can cause substrates to come loose in use although the VLSI/VHSIC microcircuit "as made" passed centrifuge testing.
 - 2. Stable contact resistance.
 - 3. Migration of metals.
- D. Silver - glass die-attach materials.

3.2 Thermal

- A. Heat conduction adequate to meet maximum allowable temperatures specified for the components.
- B. Compatability of coefficients of expansion of the die, attaching material, and the substrate.
- C. Voids in the attaching material causing hot spots.

3.3 Electrical

- A. Contact resistance "as made" and long term stability.

4. DETAILED REQUIREMENTS

- 4.1 Material Approval. All materials used to construct the test samples must have been approved. For example, the packages shall have passed testing of MIL-STD-883, and organics shall have passed the evaluation tests.
 - 4.1.1 Loose Particle Identification. The test shall consist of fastening a piece of transparent tape over the hole made during the water vapor test. The part is then placed on the loose particle or vibrator tester to capture the particles on the tape.

- 4.1.2 Internal Water Vapor. The parts shall have a water vapor content below 4000ppm for Class B and below 2000ppm for Class S. A water vapor reading between 4000 and 5000ppm for Class B and between 2000 and 3000ppm for Class S requires testing a second sample of four parts. Readings above 5000 ppm for Class B and 3000ppm for Class S shall require a complete re-evaluation.
- 4.1.3 Internal Visual. Particular attention will be focused on the quality of attachment material. Crazing, cracking, peeling, and recrystallization (for metallic attachment material) shall not be present. Only defects resulting from the attachment procedure shall be considered for this evaluation.
- 4.1.4 X-ray. The parts shall show evidence of good wetting with no part having less than 50 percent coverage for Class B, or less than 75 percent for Class S.

APPENDIX B

PROCEDURE NO. 2

WIRE BONDING

1. PURPOSE

The purpose of this test method is to provide a uniform procedure for evaluating wire bonding procedures for VLSI/VHSIC microcircuits and to assure that the process being evaluated will result in both satisfactory mechanical strength and adequate electrical properties throughout the life of the VLSI/VHSIC microcircuit.

2. REFERENCED DOCUMENT

The manufacturer shall have all areas of concern documented with respect to qualification.

2.1 Materials

- A. Specification control drawings and data for all materials
- B. Required incoming inspection
- C. Proper storage conditions

2.2 Processes

- A. Specifications to control critical parameters
- B. Minimum environmental conditions to assure consistent product
- C. Specifications for preventative equipment maintenance and calibration per Method 2011, MIL-STD-883 and ASTM F637-79

3 GENERAL REQUIREMENTS

All qualification limits shall, as a minimum, exceed the requirements as noted in MIL-M-38510 Appendix A, MIL-STD-833.

The reasoning is to be able to consistently produce VLSI/VHSIC and custom circuits that will meet or exceed all end product qualification, quality conformance and reliability goals.

3.1 Mechanical.

3.1.1 The critical process parameters that need to be controlled and monitored are:

- A. Ultrasonic power
- B. Times
- C. Work holder temperature
- D. Bond forces

3.2 Electrical.

3.2.1 Resistance "as made" and long term stability.

4. DETAILED REQUIREMENTS

4.1 Preconditioning of Test Samples. All devices submitted for evaluation testing shall be fully preconditioned before evaluation is started. This shall consist of the worst case combination of process steps, including allowable rework, and all screening tests. For example, if a maximum of two heat cycles are allowed for rework, part of the preconditioning shall include the time-temperature exposure equivalent to two rework cycles.

4.1.1 Material Approval. All materials used to construct the test samples shall have been approved. For example, the packages shall have passed MIL-STD-883, and organics shall have passed the evaluation tests.

4.1.2 Bonds. Bonds shall have minimum post-bake strength of at least half the value achieved for bonds evaluated at post-sealing. Method 2011, MIL-STD-883.

APPENDIX B

PROCEDURE NO. 3

CLEANING

1. PURPOSE

The purpose of this procedure is to establish controls on the cleaning process which is critical in the manufacture of VLSI/VHSIC microcircuit. Lack of proper control of the cleaning process can affect the reliability of the VLSI/VHSIC microcircuit.

2. GENERAL REQUIREMENTS

2.1 There are many cleaning processes which can be used in manufacturing:

- A. Mechanical - picking and scraping
- B. Gas - dry nitrogen blow
- C. Vapor - Freon degreaser
- D. Liquid - deionized water, freon, etc.
- E. Plasma
- F. Thermal - Vacuum Bake

2.2 Each of the processes must be controlled to avoid damage or degradation of the microcircuit. The cleaning medium must be monitored to assure that no contaminants are introduced in it. The exposure time must be controlled. A procedure must be set to monitor each cleaning process and audits must be performed frequently.

2.3 When a new cleaning process is to be incorporated into the manufacturing sequence, the process must be thoroughly tested to assure that all contamination is removed and that no residue is retained to cause latent failures. In addition, the cleaning process must be tested to assure that it does not degrade the VLSI/VHSIC microcircuit. A time limit must be established to control the maximum storage time between cleaning and the next assembly operation.

APPENDIX B

PROCEDURE NO. 4

SEALING

1. PURPOSE

The purpose of this test method is to evaluate techniques for sealing, VLSI/VHSIC microcircuit packages that will assure hermeticity and to assure that loose particles are not introduced into the VLSI/VHSIC microcircuit as a result of the sealing operation.

2. REFERENCED DOCUMENTS

The documentation required for review at the time of evaluation should include the following items as a minimum:

2.1 Materials

- A. Specification control drawings for all material
- B. Required incoming inspection
- C. Proper storage condition

2.2 Processes

- A. Specifications to control critical parameters

3. GENERAL REQUIREMENTS

3.1 Mechanical

- A. Seal integrity during lidding operations
- B. For metallic sealing material: long term crystallization effects.
- C. Loose particles generated by the sealing process
- D. Clearance inside the package

3.2 Electrical

- A. Pin-to-case or pin-to-pin short
 - 1. From excessive solder
 - 2. From small conductive particles generated by the sealing surface

4. DETAILED REQUIREMENTS

4.1 Internal Water Vapor. The parts shall have a water vapor content below 4000ppm for Class B and below 2000ppm for Class S. A water vapor reading between 4000 and 5000ppm for Class B and between 2000 and 5000ppm for Class S requires testing a second sample of four parts. Readings above 5000ppm for Class B and 3000ppm for Class S shall require a complete re-evaluation.

4.1.1 Seal: Fine and Gross Leak. Parts shall meet the hermeticity requirements of Method 1014, MIL-STD-883.

4.1.2 Lid Torque for Glass-Frit-Sealed Packages. Parts shall meet the strength requirements of Method 2024, MIL-STD-883.

APPENDIX C

CERTIFICATION OF TAPE AUTOMATED BONDING FABRICATION PROCESSES

<u>PROCESS NO.</u>	<u>CONTENT</u>
1	Passivation Evaluation & Wafer Preparation
2	Barrier & Field Metal Deposition
3	Photolithography for Bumping
4	Bump Electroplating
5	Inner Lead Bonding
6	Outer Lead Bonding
7	Package Seal

APPENDIX C

PROCESS NO. 1

PASSIVATION EVALUATION & WAFER PREPARATION

1. PURPOSE

Due to the wide variety of equipment, materials procedures and processes used in the cleaning and deposition of the films, this procedure will only detail the areas of concern associated with generic film deposition process and wafer cleaning.

2. REFERENCED DOCUMENTS

The thin film manufacturer shall have all areas of concern documented with respect to qualification. It is imperative that the documentation be detailed enough to be specific for each supplier.

2.1 Materials

- A. Specification control drawings and data for all materials
- B. Meaningful vendor qualification program
- C. Required incoming inspection
- D. Proper storage conditions

2.2 Processes

- A. Specifications and tools identified to control critical parameters
- B. Minimum environmental conditions to assure consistent product
- C. Specifications for preventative equipment maintenance and calibration

3. GENERAL REQUIREMENTS

All qualification limits shall as a minimum exceed the applicable requirements as noted in MIL-M-38510 Appendix-A, MIL-STD-883, Method 2021. The reason is to consistently provide VLSI/VHSIC and custom circuits that will meet or exceed all end product qualification, quality conformance and reliability goals.

4. DETAILED REQUIREMENTS

4.1 PASSIVATION: The first step is to verify that the wafers to be processed conform to the device type and revision as specified on the manufacturers procurement documents, because wafer bumping procedures are sensitive to process changes or revisions. If the device type and revision criteria have been met then the wafers are ready for passivation evaluation and characterization. The following parameters and conditions need to be verified:

- A. Thickness
- B. Adhesion
- C. Organic compound compatability
- D. Porosity/cracks/voids/pinholes
- E. Metallization compatability
- F. Step coverage and minimum overhang of 5 microns on each side over metal pad
- G. Documentation and storage

4.2 Wafer Preparation:

Wafers as received may have contamination on the bond pad areas. To assure reliability of TABed VLSI/VHSIC microcircuits the wafers can be cleaned by one or any combinations of the many cleaning methods.

- A. Gas - dry Nitrogen blow off
- B. Vapor - Freon degreaser
- C. Chemical - Dip in acid followed by DI water and solvent rinse
- D. Plasma

It is important to remember that the methods used for cleaning must be controlled to avoid damage or degradation to the device. The cleaning medium must be monitored to assure that no contaminants are introduced through it. Also the exposure time to the cleaning environment should be controlled. A control procedure must be set to monitor each cleaning process, to assure that all contaminants are removed and no residue is left behind to cause latent failures. A time limit must be identified and established to control the maximum storage time between cleaning and the next processing step. The wafers must be stored in an inert atmosphere.

APPENDIX C

PROCESS NO. 2

BARRIER & FIELD METAL DEPOSITION

1. PURPOSE

Due to the wide variety of equipment, materials procedures and processes used in the deposition of the films, this procedure will only detail the areas of concern associated with film deposition process. It is imperative that the documentation be detailed enough to be specific for each supplier.

2. REFERENCED DOCUMENT:

The thin film manufacturer shall have all areas of concern documented with respect to qualification. It is imperative that the documentation be detailed enough to be specific for each supplier.

2.1 Materials

- A. Specification control drawings and data for all materials
- B. Meaningful vendor qualification program
- C. Required incoming inspection
- D. Proper storage conditions

2.2 Processes

- A. Specifications and tools to control critical parameters
- B. Minimum environmental conditions to assure consistent product
- C. Specifications for preventative equipment maintenance and calibration

3. GENERAL REQUIREMENTS

All qualification limits shall as a minimum exceed the applicable requirements as noted in MIL-M-38510 Appendix-A, MIL-STD-883, Methods 2010 and 2018. The reason is to consistently provide VLSI/VHSIC and custom circuits that will meet or exceed all end product qualification, quality conformance and reliability goals.

4. DETAILED REQUIREMENTS

In order to achieve necessary film quality one must have a vacuum system that is capable of pumping to the ultra high vacuum region (1×10^{-7} to 8×10^{-8} Torr). One should be able to identify and verify that the base vacuum has been achieved and that the vacuum integrity is good, i.e. low amount of water vapor, low level of hydrocarbon contamination, no air leaks, etc. Critical machine parameters that need to be monitored and controlled are:

- A. Pressure level and composition
- B. Deposition rate
- C. Deposition pressure
- D. Deposition power level
- E. Substrate heating
- F. System cleanliness (deposit build-up)

5. BARRIER/FIELD METAL DEPOSITION

5.1 Barrier/Field metal deposition process conditions and properties that need to be verified are listed below:

- A. Basic metallurgical compatability
- B. Thickness
- C. Adhesion to bonding pad
- D. Step coverage
- E. Porosity/voids/cracks/pinholes
- F. Adhesion to bump
- G. Barrier effectiveness
- H. Stress
- I. Contact resistance
- J. Device damage due to substrate heating
- K. Device damage due to energetic deposition
- L. Storage in inert atmosphere

APPENDIX C

PROCESS NO. 3

PHOTOLITHOGRAPHY FOR BUMPING

1. PURPOSE

Due to the wide variety of equipment, materials procedures and processes this procedure will only detail the areas of concern with the generic photolithography process. It is imperative that the documentation be detailed enough to be specific for each supplier.

2. REFERENCED DOCUMENTS:

The manufacturer shall have all areas of concern documented with respect to qualification.

2.1 Materials

- A. Specification control drawings and data for all materials
- B. Meaningful vendor qualification program
- C. Required incoming inspection
- D. Proper storage conditions

2.2 Processes

- A. Specifications and tools to control critical parameters
- B. Minimum environmental conditions to assure consistent product
- C. Specifications for preventative equipment maintenance and calibration

3. GENERAL REQUIREMENTS

All qualification limits shall as a minimum exceed the applicable requirements as noted in MIL-M-38510 Appendix-A, MIL-STD-883, "Book of SEMI Standards for Photomasks 1983". The reason is to consistently provide VLSI/VHSIC and custom circuits that will meet or exceed all end product qualification, quality conformance and reliability goals.

4. DETAILED REQUIREMENTS

In the application of resist to barrier/field metallized wafer, the resist spinner should be able to dispense a controlled quantity of photoresist. It must be verified that certain critical parameters are monitored and controlled in the photolithography process so as to assure consistent resist process from wafer to wafer. Critical parameter controls to be verified are spin speed, spin time, spin ramp and acceleration, dispense time, bake time and temperature. In evaluation of the resist process the following conditions and parameters are of importance for rejection criteria.

- A. Adhesion
- B. No resist film (partial coverage)
- C. Contamination, crushed resist, smudges
- D. Orange peel
- E. Thickness
- F. Comets, drops of resist, strain on surface

5. ALIGN, EXPOSE & DEVELOP

Prior to wafer alignment and exposure verify that a procedure exists to insure the correct mask and revision are used. The quality of the photomask will be per SEMI standards. The mask shall be checked for contamination, scratches and other irregularities which will effect the quality of photoresist. Monitoring of the uniformity of the exposure energy over the entire wafer region, must be verified as well as parameters critical to resist development including temperature and developer uniformity (mild agitation or spray coverage). Verify that after developing the wafer is inspected for the following:

- A. Double images
- B. Voids resist or extraneous defects caused by scratches or mask contact problems, contamination, spiking on wafer, step coverage problems
- C. Lifting resist
- D. Under exposure
- E. Over exposure
- F. Alignment accuracy
- G. Edge profile (pattern definition)
- H. Poorly developed pattern

APPENDIX C

PROCESS NO. 4

BUMP ELECTROPLATING

1. PURPOSE

Due to a variety of equipment, materials procedures and processes used in the plating of bumps on pad areas this procedure will detail the areas of concern with a generic plating process. It is imperative that the documentation be detailed enough to be specific for each supplier.

2. REFERENCED DOCUMENTS:

The manufacturer shall have all areas of concern documented with respect to qualification.

2.1 Materials

- A. Specification control drawings and data for all materials
- B. Meaningful vendor qualification program
- C. Required incoming inspection
- D. Proper storage conditions

2.2 Processes

- A. Specifications and tools to control critical parameters
- B. Minimum environmental conditions to assure consistent product
- C. Specifications for preventative equipment maintenance and calibration

3. GENERAL REQUIREMENTS

All qualification limits shall as a minimum exceed the applicable requirements as noted in MIL-M-38510 Appendix-A, MIL-STD-883. The reason is to consistently produce TABed VLSI/VHSIC and custom circuits that will meet or exceed all end product qualification, quality conformance and reliability goals.

AD-A164 885

QUALITY PROCEDURES FOR VLSI/VHSIC (VERY LARGE SCALE
INTEGRATED AND VERY H. (U) ITT ADVANCED TECHNOLOGY
CENTER SHELTON CT S COHEN NOV 85 RADC-TR-85-219

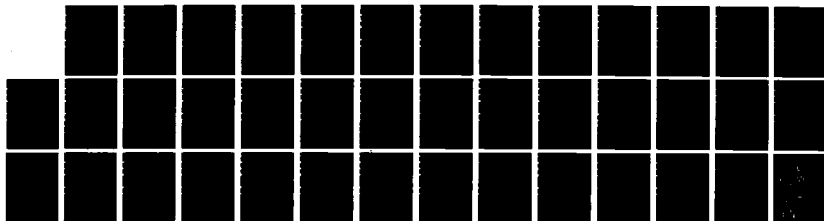
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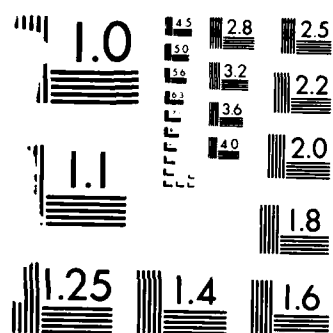
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

4. DETAILED REQUIREMENTS

Prior to plating verify existence of an inspection with Accept/Reject criteria for using a UV-fluorescence microscope (30 X to 60 X) to sample each lot to assure that the photoresist has completely developed from the bond pad areas and that no organic residue resides where plating is to be accomplished. Verify that the critical parameters to be monitored and controlled for the plating are:

- A. Plating solution flow rate
- B. Current density
- C. Plating solution temperature
- D. Plating solution specific gravity
- E. Plating solution pH level
- F. Level of impurities (particularly organic)

To assure the quality of the bump plating itself verify specifications, controls and tests for the following:

- A. Bump height, uniformity
- B. Bump size and shape
- C. Bump grain structure
- D. Bump hardness
- E. Min. bump to bump spacing (mushrooming)
- F. Bump shear (adhesion)
- G. Contamination on bump surface
- H. Extraneous plating patches

APPENDIX C

PROCESS NO. 5

INNER LEAD BONDING

1. PURPOSE

Due to a variety of equipment, materials procedures and processes used in assembly of VLSI/VHSIC microcircuits, this procedure will detail the areas of concern associated with generic inner lead bonding. It is imperative that the documentation be detailed enough to be specific for each supplier.

2. REFERENCED DOCUMENTS:

The manufacturer shall have all areas of concern documented with respect to qualification.

2.1 Materials

- A. Specification control drawings and data for all materials
- B. Required incoming inspection
- C. Proper storage conditions

2.2 Processes

- A. Specifications and tools to control critical parameters
- B. Minimum environmental conditions to assure consistent product
- C. Specifications for preventative equipment maintenance and calibration per Method 2011, MIL-STD-883; ASTM F637-79.

3. GENERAL REQUIREMENTS

All qualification limits shall as a minimum exceed the applicable requirements as noted in MIL-M-38510 Appendix-A, MIL-STD-883. The reason is to consistently produce TABed VLSI/VHSIC and custom circuits that will meet or exceed all end product qualification, quality conformance and reliability goals.

4. DETAILED REQUIREMENTS

TAPE INSPECT: Verify that prior to the inner lead bonding of devices a visual inspection of the TAB tape should be performed. The Accept/Reject criteria for inspection shall be based on the following:

- A. Lead width
- B. Surface contamination
- C. Plating defects
- D. Mechanical damage to leads
- E. Storage in dry inert atmosphere

5. INNER LEAD BONDING

Verify that the following critical process parameters are controlled and monitored for inner lead bonding.

- A. Tape tension
- B. Thermode dwell time
- C. Approach pressure
- D. Bond pressure
- E. Pedestal temp
- F. Thermode temp
- G. Thermode/pedestal planarity
- H. Correct beam on bump placement

Verify that the manufacturer has optimized his bonding parameters and developed specifications to take into account variations in:

- A. Chip size
- B. Lead count
- C. Bump size
- D. Metallization system used (both bump and tape beams)
- E. Bump hardness
- F. Bump center distances
- G. Attachment material under die

Verify that the manufacturer has qualified his inner lead bond metallization system (e.g. barrier metal, electroplated bump, plated tape lead) by extended stressing and life testing at temperatures of 250°C for 1000 hours with no more than 30% beam to chip pull strength degradation.

APPENDIX C

PROCESS NO. 6

OUTER LEAD BONDING

1. PURPOSE

Due to a variety of equipment, materials procedures and processes used in the outer lead bonding of VLSI/VHSIC microcircuits, this procedure will detail the areas of generic concern. It is imperative that the documentation be detailed enough to be specific for each supplier.

2. REFERENCED DOCUMENTS:

The manufacturer shall have all areas of concern documented with respect to qualification.

2.1 Materials

- A. Specification control drawings and data for all materials
- B. Meaningful vendor qualification program
- C. Required incoming inspection
- D. Proper storage conditions

2.2 Processes

- A. Specifications and tools to control critical parameters
- B. Minimum environmental conditions to assure consistent product
- C. Specifications for preventative equipment maintenance and calibration

3. GENERAL REQUIREMENTS

All qualification limits shall as a minimum exceed the applicable requirements as noted in MIL-M-38510 Appendix-A, MIL-STD-883. The reason is to consistently produce TABed VLSI/VHSIC and custom circuits that will meet or exceed all end product qualification, quality conformance and reliability goals.

4. DETAILED REQUIREMENTS

PACKAGE INSPECTION Verify that prior to outer lead bonding a flatness screen of the entire package and the cleaning of the same is carried out. The criteria for inspection shall be based on the following:

- A. Package flatness
- B. Uniformity of thickness of outer leads

Verify that packages are thoroughly cleaned to remove any organic contamination to assure that a reliable tape to package foot bond will be achieved. The critical process and/or machine parameters that need to be monitored and controlled to consistently produce good bonds are:

- A. Thermode dwell time
- B. Bond pressure
- C. Approach pressure
- D. Pedestal temperature
- E. Thermode temperature
- F. Trim and form regularity
- G. Planarity of thermode and package pedestal
- H. Accuracy in beam to foot placement
- I. Degredation of inner lead bond

Verify that the manufacturer has optimized his outer lead bonding parameters and developed specifications to take into account variations in:

- A. Package size and geometry
- B. Package material
- C. Lead count
- D. Type of tape
- E. Tape plating types
- F. Planarity of package

Verify that the manufacturer has qualified his outer lead bond metallization scheme to give a tape beam to package foot bond that does not fail (bond strength degradation greater than 30%) after 250°C and 1000 hours life test. Also that the outer process does not degrade the inner lead bond.

APPENDIX C

PROCESS NO. 7

SEALING

1. PURPOSE

The purpose of this test method is to evaluate techniques for sealing, VLSI/VHSIC microcircuit packages that will assure hermeticity and to assure that loose particles are not introduced into the VLSI/VHSIC microcircuit as a result of the sealing operation.

2. REFERENCED DOCUMENTS

The documentation required for review at the time of evaluation should include the following items as a minimum:

2.1 Materials

- A. Specification control drawings for all material
- B. Required incoming inspection
- C. Proper storage condition

2.2 Processes

- A. Specifications to control critical parameters

3. GENERAL REQUIREMENTS

3.1 Mechanical

- A. Seal integrity during lidding operations
- B. For metallic sealing material: long term crystallization effects.
- C. Loose particles generated by the sealing process
- D. Clearance inside the package

3.2 Electrical

- A. Pin-to-case or pin-to-pin short
 - 1. From excessive solder
 - 2. From small conductive particles generated by the sealing surface

4.DETAILED REQUIREMENTS

- 4.1 Internal Water Vapor. The parts shall have a water vapor content below 4000ppm for Class B and 2000ppm for Class S. A water vapor reading between 4000 and 5000ppm for Class B and between 2000 and 5000ppm for Class S requires testing a second sample of four parts. Readings above 5000ppm for Class B and 3000ppm for Class S shall require a complete re-evaluation.
- 4.1.1 Seal: Fine and Gross Leak. Parts shall meet the hermeticity requirements of Method 1014, MIL-STD-883,
- 4.1.2 Lid Torque for Glass-Frit-Sealed Packages. Parts shall meet the strength requirements of Method 2024, MIL-STD-883.

APPENDIX A4

CERTIFICATION REQUIREMENTS FOR
VLSI MICROCIRCUITS, FACILITIES AND LINES

PROPOSED MIL-STD 17XX
"CERTIFICATION REQUIREMENTS FOR
VLSI MICROCIRCUITS
FACILITIES AND LINES"

MIL-STD-XXXX

FORWARD

The purpose of this standard is to establish criteria for certification (as required by MIL-M-38510) of lines and facilities for the manufacture of Very Large Scale Integration (VLSI) microcircuits. For the purpose of this document, VLSI monolithic microcircuits are defined as devices with photolithographically defined circuit features equal to or less than 3 microns that have more than 10,000 logic gates. The criteria defined herein are intended as a prerequisite for qualification of Class B and Class S Very Large Scale Integration (VLSI) Circuits.

1.0 SCOPE

- 1.1 Purpose. This standard establishes the minimum requirements for the certification of manufacturing lines/facilities used in fabrication of high reliability Very Large Scale Integration (VLSI) Circuits.
- 1.2 Application. The requirements of this standard apply to both CUSTOM and JAN VLSI circuits (as defined herein). It applies to Class B and Class S microcircuits in packaged and dice form.

2.0 REFERENCED DOCUMENTS

- 2.1 Government Documents The following documents form a part of this standard to the extent specified herein:

Military
MIL-M-38510
Standards
Federal
FED-STD-209

Military
MIL-STD-883
MIL-STD-976A
MIL-STD-977
MIL-STD-45662

- 3.0 DEFINITIONS The following definitions apply in addition to those definitions specified in MIL-M-38510.

Certification Team The contracting officer's designated representative(s) responsible for auditing the manufacturers capabilities of supplying high-reliability custom, or JAN, VLSI circuits.

Custom VLSI Microcircuits A custom Very Large Scale Integrated circuit is a non-standard (not covered by a MIL-M-38510 detail specification) monolithic VLSI which is designed and manufactured for a specific system application.

4.0 GENERAL REQUIREMENTS

4.1 Certification Requirements

The following requirements are applicable to the certification of VLSI circuit manufacturing lines/facilities:

- 4.1.1 Verification (by audit) of the manufacturer's quality program for conformance with MIL-M-38510 Appendix A requirements.
- 4.1.2 Verification of the manufacturer's process capability. Manufacturers must demonstrate that their wafer fabrication process(es) and line(s) can consistently produce the VLSI circuit geometries and electrical parameters defined in the design rules for the process(es) to be certified.
- 4.1.3 Verification of the manufacturer's assembly, test, screening, analytical capability. Manufacturers must demonstrate that they have (or can effectively manage) the facilities required to assemble, test, screen, analyze VLSI circuits for high-reliability military systems.

5.0 DETAILED REQUIREMENTS

5.1 Pre-survey Requirements

- 5.1.1 Manufacturers shall submit data to the certifying authority in sufficient detail to allow evaluation of his capability to meet the certification requirements: The pre-audit data required is listed in Table I.

TABLE I

REQUIREMENT	DATA TO BE SUBMITTED
Prior VLSI manufacturing experience	Production, test, screening, reliability data on product of similar complexity, design rules, technology, as the devices for which certification is requested. (Data taken on process validation modules/test chips for the process to be certified may be used.)
Compliance with MIL-M-38510, Appendix A Product Assurance requirements	Product Assurance Program plan, facilities (wafer fabrication, assembly, test, analytical) description
Process capability demonstration	Application design rules, description of process validation module/test chip, process and test device parameters, wafer lot acceptance data (ref: Method 5007, MIL-STD-883) from similar process/design rules)

5.1.2 Facilities Description

Facilities description shall include:

- 5.1.2.1 Monitoring and controls on particle count, temperature, humidity in critical process areas (photolithography, diffusion, oxidation, ion implant).
- 5.1.2.2 Wafer control - Monitoring and controls on resistivity, organic impurities, bacteria count, solids content.

- 5.1.2.3 Gas controls - Moisture monitoring and control.
- 5.1.2.4 Monitoring and calibration of computer-controlled processes (ion implant, diffusion, oxidation, et al).
- 5.1.2.5 Listing of in-house capabilities for device testing, mechanical and environmental screening, calibration, destructive physical, chemical, failure analysis.

5.1.3 Process Capability Demonstration

To assist the survey team in evaluating the vendor's process, the following information will be required prior to the audit:

- 5.1.3.1 Electrical and process parameters, test conditions, accept/reject criteria for the process validation device.
- 5.1.3.2 Reliability test data applicable to the process/line to be certified. This could include results of metal stability, metal integrity, contact integrity, contact-resistance stability, accelerated life tests, dielectric stress tests.
- 5.1.3.3 Measurement and control of defect density. Methods used for monitoring process-induced defects. Supporting data for claimed defect density. Procedures for defect density control.

5.2 Survey Requirements

5.2.1 Test Structures (PCM)

On-site evaluation will be performed on the vendor's use of test structures for measuring process performance and control. Methods for verifying the process and design parameters shall be demonstrated to the audit team members. If the device procurement specification permits use of stress-and-test

techniques on surrogate (test) chips in lieu of 100% high-magnification die inspection, these procedures shall be demonstrated. Where the vendor's photolithographic techniques do not permit inspection of test chips in product wafers, the use of Process Validation Wafers (wafers containing only test patterns) for process control, defect or yield monitoring and product lot acceptance shall be demonstrated. Test wafers used for lot acceptance testing must be processed simultaneously with the product wafers through the critical process steps (oxidation, diffusion, ion implant, contact, reflow, metallization).

5.2.1.1 Test Structure Requirements

The test structures shall contain test devices/patterns to verify the process, design, reliability parameters listed in Table I. The design rules for the test structures shall be identical to the VLSI specification, or mutually agreed upon by the design and fabrication facilities.

5.2.2 Facilities/Lines Audit

The certification team will audit the manufacturer's facilities/lines to verify that the controls imposed on manufacturing, inspection, and testing are sufficient to assure conformance with MIL-M-38510 requirements, this standard, and the device specification.

5.2.2.1 Facilities Audit

The facilities audit requirements are listed in Appendix A. The appraisal forms will be completed by the survey team and observations discussed with the manufacturer's representatives at the conclusion of the audit.

VLSIC MANUFACTURING FACILITIES/LINES SURVEY
SUMMARY REPORT

Date(s) of Survey:	Wafer Fabrication	Assembly & Packaging
Company Name:	Facility Location(s)	
Product(s) Technology:	Minimum Feature Size:	microns

Recommendations:	Approved Approved subject to satisfactory audit of Corrective actions Not Approved
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<u>Summary of Observations</u>	Acceptable	Not Acceptable	Reference Numbers for Observations
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1. Organization
2. Building & Services
3. Operator Training & Certification
4. Process Documentation
5. Maintenance & Calibration Procedure
6. Material Controls/Storage
7. Quality Control
8. Wafer Fabrication Line
9. Assembly & Packaging Line
10. Process Controls
11. Acceptance Tests
12. Configuration Management
13. Clean Room Disciplines
14. CAM

Equipment	Manufacturing Inspection Testing Screening Analytical
-----------	-------------------------------------------------------------------

VLSIC MANUFACTURING FACILITIES/LINES SURVEY
NON-CONFORMING DETAIL REPORT

Date(s) of Survey: Wafer Fabrication Assembly & Packaging
Supplier Name: Facility Location(s)

Ref. No. Observations

Supplier Representatives:

Audit Team Members:

Facilities Appraisal, Element #1

Organization

Requirement: The device manufacturer's organization should include technical interfaces between the manufacturing staff (wafer fabrication, assembly, test), the device design activity and the contractor (user). This interface (normally a product engineering function) shall have the expertise to distinguish between design/fabrication/test-related device yield problems.

The interfaces of the suppliers project team members with the design and applications organizations should be shown on the organization chart.

Reference: None

Audit

1. Organization Chart (Project Organization)
2. Prior VLSI Project Experience
3. Manufacturing Organization
(Relationships/authorities of manufacturing, engineering, test, QA)

Facilities Appraisal, Element #2

Building and Services

Requirement: The building and services must be capable of supporting the requirements for reproduceable and reliable manufacture of VLSI product.

Reference: FED-STD 209

Audit:

1. Wafer fabrication and assembly layout
2. Controlled environment specifications (temperature, humidity, dust count, air flow) in wafer fabrication and assembly areas
3. Deionized water facilities and specifications
4. Monitoring and control facilities for deionized water, air, gases, chemicals
5. Equipment support services (set-up maintenance, calibration, test)

Facilities Appraisal, Element #3

Operator Training and Certification

Requirement: Personnel performing critical wafer fabrication and assembly operations must be trained and certified in accordance with documented criteria.

Reference: MIL-M-38510, Appendix A, 20.1.1.2, 20.1.2.1

Audit:

1. Training program content, documentation
2. Operator training/certification records
3. Decertification/retraining procedures

Facilities Appraisal, Element #4

Process Documentation

Requirement: All wafer fabrication and assembly processes must be performed in accordance with documented work instructions. These instructions must also include set-up, maintenance, and operation of process equipment, operating and ambient conditions.

The baseline process flow sequence for the specific VLSI(s) to be manufactured shall be part of the process documentation. In addition to the requirements in Par. 20.1.3.2, the flow sequence shall include starting material requirements, critical process parameters and measurement limits (such as: dielectric and metal thicknesses; furnace temperatures, times, gas flow rates; ion implant energies, doses, dopant species; junction depths; surface concentrations, sheet resistivities, device vertical and lateral dimensions).

Reference: MIL-M-38510, Appendix A, Sections 20.1.1.6, 20.1.3.2

Audit:

1. Baseline process documentation
2. Document control procedures, records
3. Lot travelers/lot process records
4. Revision status of operator instructions

Facilities Appraisal, Element #5

Maintenance and Calibration Procedures

- Requirement:
1. Tool, gauge and test equipment maintenance and calibration shall comply with Par. 20.1.1.9 requirements.
 2. Equipment calibration shall comply with Par. 20.1.2.5 requirements
 3. The requirements for Par. 20.1.1.9 (for documented procedures and frequency of scheduled actions) shall also apply for equipment whose calibration and maintenance are critical for VLSI process control (ion implanters, furnace systems for gate oxidation/diffusion/polysilicon, reactive ion etchers, photoresist spinners, photon and electron beam alignment and exposure systems, D.I. water system)
- References:
- MIL-M-38510, Appendix A
MIL-STD-45662
- Audit:
1. Procedures for set-up maintenance, calibration of process-critical equipment
 2. Equipment logs (ion implanter, furnaces) for conformance to procedures
 3. Verify procedures for calibration of closed-loop, computer-controlled furnaces (methods, frequency for verifying temperature profile, gas flow rates, C-V plots)
 4. Ion implant dosimetry calibration
 5. Calibration procedures/standards for dielectric polysilicon thickness, junction depth measurement.

Facilities Appraisal, Element #6

Material Controls/Storage

Requirement: 1. The methods for controlling incoming, in-process and completed inventory shall be in accordance with Paragraph 20.1.1.12

Reference: MIL-M-38510, Appendix A

Audit:

1. Identification of in-process wafer lots
2. Staging areas for photo steps, active mask inventory
3. Storage and identification of non-conforming material
4. Finished goods inventory
5. Storage of package assembly material (packages, lids, preforms, adhesives)
6. Maximum wafer hold periods for critical process steps
7. Wafer trail from receipt through inspection, starting wafer inventory, production control, starting wafer lot formation
8. Photoresist storage, dispensing, dating

Facilities Appraisal, Element #7

Quality Controls

Requirement: The manufacturer must perform sufficient inspections and tests on incoming, in-process, and finished material to insure that the VLSIs meet the requirements of this standard. The referenced MIL-M-38510 paragraphs and the applicable detailed specification. The inspections and tests must be identified on the process baseline documentation. Production and quality assurance personnel performing inspection functions must have been trained and certified to perform their assigned task(s) in accordance with the in-house procedures.

Reference: MIL-M-38510 Paragraphs 4.1, 4.2, 4.3

Audit:

1. Incoming inspection procedures (wafers, packages, photoresist, masks), inspection records
2. In-process, final visual wafer inspections, accept-reject criteria, inspection operator certification
3. Pre-seal vision inspection (Production & QA), operator training and certification
4. SEM inspection, operator training & certification
5. Wire-bond, die-attach inspections, tests

Facilities Appraisal, Element #8

Wafer Fabrication Line

Requirement: The wafer fabrication line, which includes processing, process monitoring, wafer electrical test, and inspection equipment, the environmental controls (air temperature, humidity, pressure, cleanliness) must be capable of producing wafers with defect densities consistent with the VLSI design rules and complexity.

Reference: Federal Standard 209

- Audit:
1. Use of CAM equipment for critical wafer processes
 2. Air flow rates, particle control in critical wafer processing areas; monitoring and alarm systems
 3. Clean room specifications
 4. Personnel access controls: air-locks, gowning areas
 5. General cleanliness (clean room disciplines) in wafer fabrication line
 6. Wafer handling and storage facilities - non-manual wafer handling, electrostatic-damage controls (uniforms, flooring, equipment)
 7. Wafer flow.

Facilities Appraisal, Element #9

Assembly and Packaging Line

Requirement: The assembly and packaging line, which includes assembly, assembly monitoring, inspection, mechanical and environmental test equipment, environment controls (air temperature, humidity, cleanliness) must be capable of producing high-reliability packaged VLSI circuits meeting the requirements for Class "B" or Class "S", as applicable.

Reference: Federal Standard 209
Method 5004, MIL-STD 883
MIL-M-38510, Paragraph 4.6

- Audit:
1. Die-separation, die-attach, die-package interconnection, package sealing, die-clean equipment and controls, control charts, corrective actions
 2. Pre-seal visual inspection station(s)
 3. Screening equipment & procedures
 4. Air monitoring and controls
 5. Sub-assembly storage facilities (ambient controls)
 6. Lot travellers
 7. Operator training and certification
 8. Process controls on die attach and interconnect (wire-bonding, tape-automated-bonding, other)
 9. Internal (package) moisture, contamination controls

Facilities Appraisal, Element #10

Process Controls

Requirement: The wafer fabrication, assembly and packaging, test operations shall have sufficient process controls to insure reproducibility of the baseline processes. These process controls shall include process validation chips (or wafers), control charts/wafers, visual inspection, C-V plots, SEM inspection, destructive physical analysis.

The manufacturer shall demonstrate the use of test chips and/or process validation wafers for verification of the specified process and design parameters.

Reference: MIL-STD-977

- Audit:
1. Manufacturer's verification of process/design parameters, process-induced defects, dielectric/metal integrity using test chips, process validation on wafers
 2. Control charts, corrective actions on critical processes
 3. Procedures for verifying critical vertical and lateral dimensions
 4. Use of SEM for process control and metal inspection
 5. Verification of metallization and contact reliability
 6. Wafer visual inspections
 7. Use of surrogate chips/wafers for lot acceptance

Facilities Appraisal, Element #11

Acceptance Tests

Requirement: The manufacturer must be capable of performing all required acceptance tests. If testing is sub-contracted, the manufacturer shall show data demonstrating capability to provide technical and management support.

1. Wafer lot acceptance
2. Post-assembly screening
3. Radiation (if required by detailed specification)
4. Lot conformance
5. Wafer probe
6. Final electrical

Reference: Method 5007, MIL-STD 883
Method 5010, MIL-STD 883

Audit:

1. Wafer lot acceptance records, procedures for conformance to requirements
2. Burn-in and final test procedures
3. Wafer probing operation, including high/low temperature test capabilities
4. Facilities for conducting/managing radiation-hardness assurance testing (if applicable)
5. Burn-in/life test facilities, procedures
6. Lot conformance tests (metallization, contact, dielectric integrity)
7. Final electrical tests
8. Failure analysis procedures

Facilities Appraisal, Element #12

Configuration Management

Requirement: The VLSI manufacturer must have an effective configuration management system for the control of the manufacturing baseline, process, assembly and test documentation. In addition, the manufacturer's configuration control system must insure correct revision status of VLSI device design (including mask tooling) test documentation, package pinout, and system specifications.

Reference: None

Audit:

1. Methods and procedures for implmentation and control of changes in VLSI device design, mask tooling, material, processing and testing
2. Control of changes in CAM equipment
3. Procedures for verification of the baseline device configuration on initial lot conformance inspection
4. Procedures for release and verification of wafer probe and final test programs
5. Specification drawing change control

Facilities Appraisal, Element #13

Clean Room Discipline

Requirement: Clean room discipline is an essential part of manufacturing process control required for economic and reliable VLSI production. Documented procedures must be established and maintained for control of personnel access, proper use and periodic cleaning of clean room attire, incoming material and equipment cleanliness, printed matter, paper, packaging material, writing material, facility cleaning procedures.

Reference: None

- Audit:
1. Control and shutdown limits for dust count
 2. General cleanliness of clean room(s)
 3. Use of lint-free paper for all printed matter (log books, control charts, printers, process instructions, lot travellers)
 4. Procedures for cleaning incoming material, supplies, equipment
 5. Dust isolation controls (air locks, gowning areas, use of sticky mats, shoe brushes)
 6. Controls on visitors and outside contractors attire and conduct in clean room areas
 7. Hair, hand, face covering by operators and supervisors
 8. Manual wafer/mask handling procedures (if used)
 9. Clean room specifications/procedures

APPENDIX B

CAM FACILITIES AND PROCESS CONTROLS,

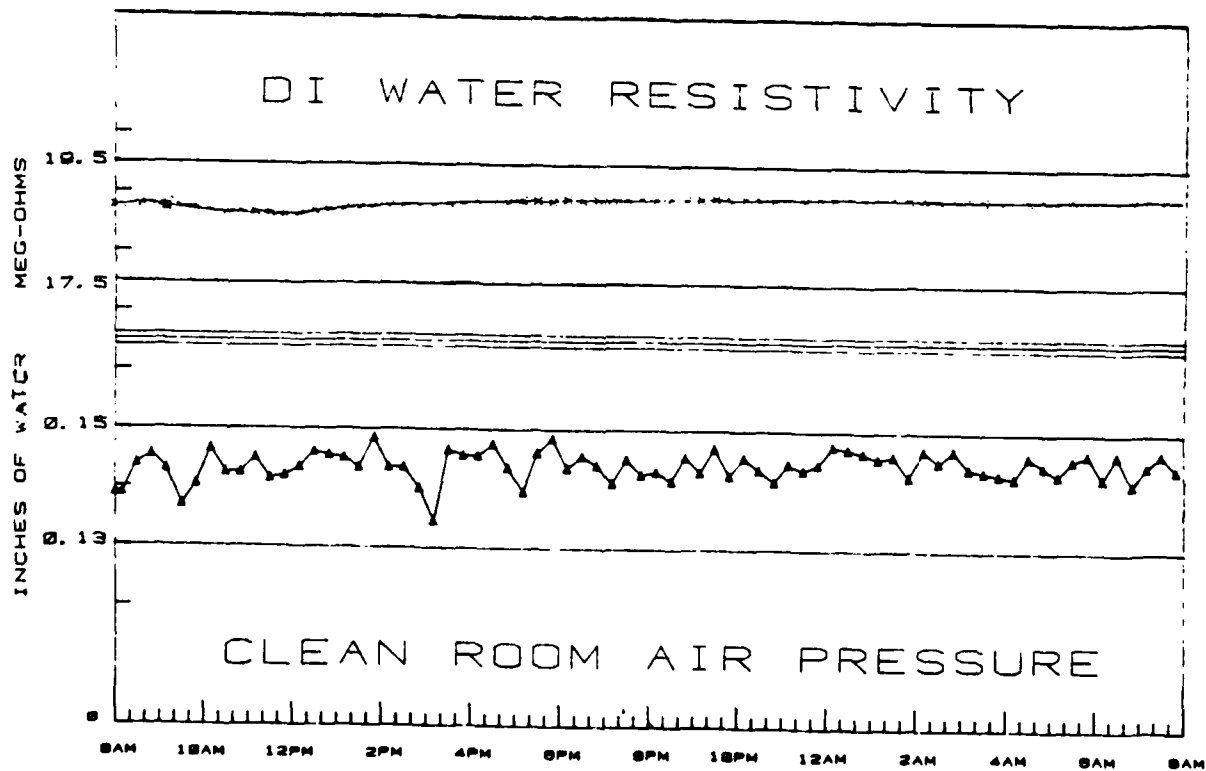
EXAMPLES:

- B1 - DI Water Resistivity
- B2 - Clean Room Humidity
- B3 - Daily Printout, Facilities
- B4 - Printout, Computerized Material Review Program
- B5 - Wafer Tracking System Data Summary
- B6 - Equipment History Report
- B7 - WTS Computer-Generated Major Step Traveller

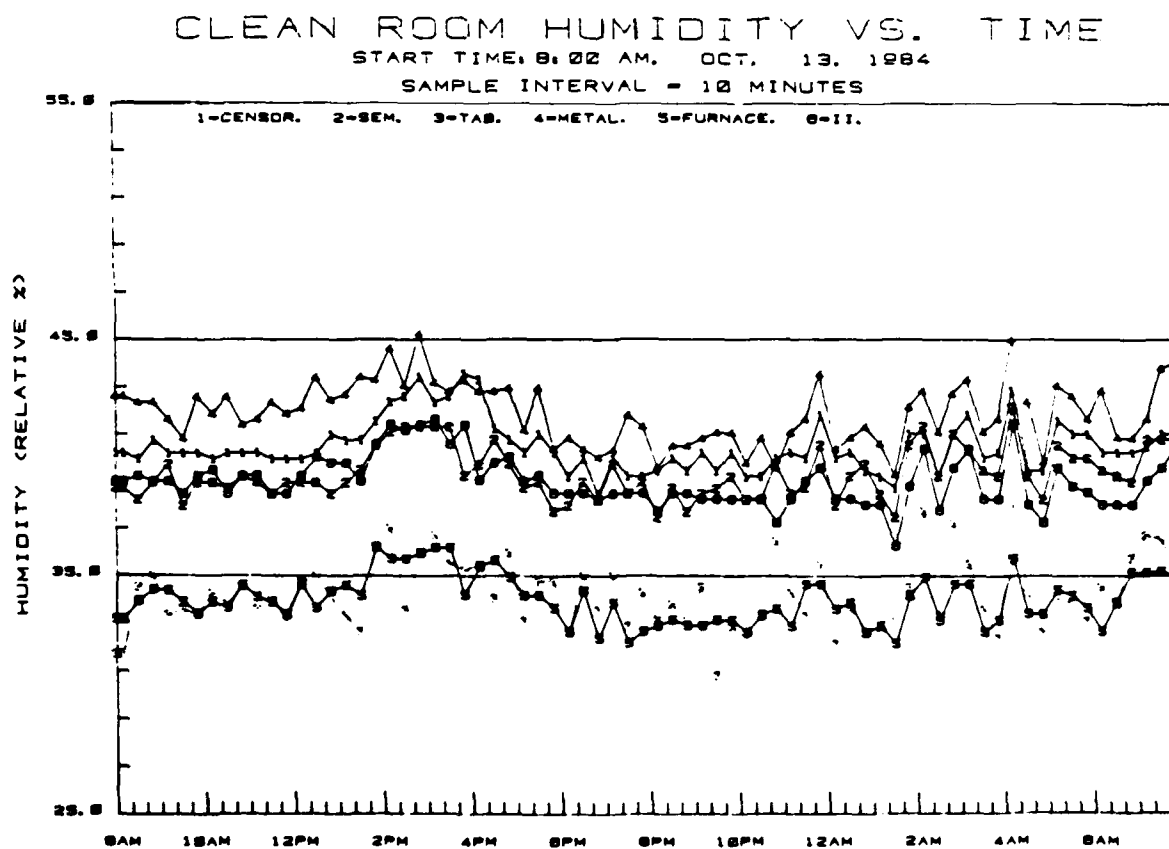
B1 - DI WATER RESISTIVITY

ITT VLSI FABRICATION FACILITY MONITORING

START TIME: 8:00 AM. OCT. 13, 1984



B2 - CLEAN ROOM HUMIDITY



B3 - DAILY PRINTOUT, FACILITIES

ITT VLSI FABRICATION FACILITY MONITORING

START TIME : 8:00 AM, OCT. 13, 1984, FOR 24 HRS AVERAGE.

NUMBER OF MEASUREMENTS FOR THIS REPORT = 144

TEMPERATURE (Degree F)

LOCATION	MEAN	SIGMA	MINI	MAXI	OUT-OF-LIM(%)
1 CENSOR	68.509	.2429	67.259	68.737	4.86
2 SEM	69.049	.2903	68.441	69.918	0.00
3 TAB	70.848	.4574	69.918	71.981	0.00
4 METAL	69.442	.5481	68.146	70.803	0.00
5 FURNACE	74.440	.5296	73.159	75.802	0.00
6 II	69.924	.2943	69.328	71.392	0.00

HUMIDITY (Rel. %)

LOCATION	MEAN	SIGMA	MINI	MAXI	OUT-OF-LIM(%)
1 CENSOR	40.523	1.1152	38.441	43.570	0.00
2 SEM	39.354	1.1291	37.210	42.946	0.00
3 TAB	34.382	1.3909	30.812	39.073	68.75
4 METAL	41.953	1.3209	39.251	45.258	2.08
5 FURNACE	34.084	1.0176	32.168	36.510	79.86
6 II	38.996	1.1244	36.247	41.642	0.00

PRESSURE (Inch of H2O)

LOCATION	MEAN	SIGMA	MINI	MAXI	OUT-OF-LIM(%)
CLASS-100	.1438	.0030	.1215	.1490	0.00
AIR LOCK	.1040	.0039	.0863	.1238	.69
CLASS-10K	.1044	.0037	.0895	.1110	0.00
PR-FILTER	.5048	.0057	.4920	.5174	0.00
HEPA-B ARE	.9412	.0055	.9154	.9524	4.86
MEN GOWN	.1041	.0049	.0723	.1242	1.39

DI WATER LOOP-RES. (MegOhm)

LOCATION	MEAN	SIGMA	MINI	MAXI	OUT-OF-LIM(%)
1	18.87	.11	18.62	18.99	0.00

B4 - PRINTOUT, COMPUTERIZED MATERIAL REVIEW PROGRAM

MRE number is: 751
Lot number is: 4508
Process ID is: 5NMOSH
Number of wafers is: 71
Wafers scrapped are: 1
Wafers reworked are: 17
Wafers waived are: 73
Major step code is: 4014
Minor step code is: S4209
Discrepancy code is: 0
Date is: Jan., 23, 1985
Discrepancy is: 74 WFS ARE OK (CONTACTS OPEN DOWN TO SILICON) 17 WFS U
NDERETCHED... (P.S... RESIST NOT STRIPPED)
Possible cause is: OX, THICK, NOT UNIFORM FROM WFR. TO WFR.
Actual cause is: SAME AS POSSIBLE CAUSE.
Preventive action: EVALUATE PSG DEP. AND UNIFORMITY.
Rework instructions: RETCHED TO COMPLETION, DONE BY ENG.
Entered by: 2424
Dispositioned by: 2805

B5 - WAFER TRACKING SYSTEM DATA SUMMARY

*
* WTS MEASUREMENT DATA SUMMARY *
*

Report Time: 2:42 PM TUE., 12 MAR., 1985
Process id : 5CM0SG
Major Step : LOMAC TEST ...83038353
Minor Step : Input Vtn Average , Spec = .40 Volts-- 1.10 Volts
LOT-ID DEVICE-ID OPER min mean max sigma DATE

445Q	CSSC06	2307	.86,	.86,	.86,	0.00	01/11/85
445C	CSSC06	2307	.90,	.90,	.90,	0.00	01/11/85
446F	CSSC06	2307	.85,	.85,	.85,	0.00	01/15/85
449B	CSSC06	2307	.94,	.94,	.94,	0.00	01/17/85
445M	CSSC06	2307	.90,	.90,	.90,	0.00	01/17/85
446G	CSSC06	2307	.89,	.89,	.89,	0.00	01/19/85
446I	CSSC06	2307	.86,	.86,	.86,	0.00	01/19/85
4450	CSSC06	2307	.83,	.83,	.83,	0.00	01/23/85
443A	CSSC06	2307	.98,	.98,	.98,	0.00	01/23/85
447G	CSSC06	2307	.96,	.86,	.86,	0.00	01/24/85
448D	CSSC06	2307	.85,	.85,	.85,	0.00	01/24/85
448E	CSSC06	2307	.95,	.95,	.95,	0.00	01/24/85
446H	CSSC06	2307	.85,	.85,	.85,	0.00	01/25/85
448A	CSSC06	2307	.85,	.85,	.85,	0.00	01/25/85
448B	CSSC06	2307	.90,	.90,	.90,	0.00	01/29/85
447K	CSSC06	2307	0.00,	0.00,	0.00,	0.00	02/06/85
502D	CSSC06	2491	.86,	.86,	.86,	0.00	02/23/85

MIN VALUE 0.00 MAX VALUE98
MEAN VALUE83 SIGMA VALUE 0.00
PERIOD DATA TAKEN...FROM 01/11/85 TO 02/23/85

0.00 1.10

445Q	\$	*	\$
445C	\$	*	\$
446F	\$	*	\$
449B	\$	*	\$
445M	\$	*	\$
446G	\$	*	\$
446I	\$	*	\$
4450	\$	*	\$
443A	\$	*	\$
447G	\$	*	\$
448D	\$	*	\$
448E	\$	*	\$
446H	\$	*	\$
448A	\$	*	\$
448B	\$	*	\$
447K	\$	*	\$
502D	\$	*	\$

B6 - EQUIPMENT HISTORY REPORT

MACHINE HISTORY REPORT.

PERIOD IS FROM 4/15/84 TO 4/21/84

Mach.	Description	Time down	Time up	Down time	Reason Code	Page 2
2542	BRUCE 42 NITRIDE DEP	APR. 17 at 12:11	APR. 17 at 12:45	0:44	11	
				Total down time: 0:44		
				Availability was 99.67		
2543	BRUCE 43 POLY DEP	had no down time during this period.				
2544	BRUCE 44 BARRIER INT	had no down time during this period.				
2551	BRUCE 51 S/D DIFF	had no down time during this period.				
2552	BRUCE 52 ACS LTO	had no down time during this period.				
2553	BRUCE 53 REFLOW	had no down time during this period.				
2554	BRUCE 54 POCL3 DEP	had no down time during this period.				
2561	ANT HIPOX OX SYSTEM	had no down time during this period.				
2562	DUMP TRANSFER 1	had no down time during this period.				
2563	DUMP TRANSFER 2	had no down time during this period.				
2564	DUMP TRANSFER 3	had no down time during this period.				
2565	DUMP TRANSFER 4	had no down time during this period.				
3501	CF-4 ION IMPLANTER	had no down time during this period.				
3502	MPC R1-151 SPUTTER	MFR. 17 at 8:00 APR. 17 at 8:40		0:40	11	
3502	MPC R1-151 SPUTTER	APR. 17 at 13:00 APR. 18 at 11:00		22:00	12	
3502	MPC R1-151 SPUTTER	APR. 18 at 11:00 APR. 19 at 10:00		23:00	13	
				Total down time: 45:40		
				Availability was 72.60		
3503	MPC GOLD PAD SPUTTER	APR. 17 at 9:30	APR. 19 at 16:30	55:00	11	
				Total down time: 55:00		
				Availability was 67.33		
3504	MPC WAFERLINE	had no down time during this period.				
3505	120-10 ION IMPLANTER	had no down time during this period.				
3506	Edwards CV Evap	had no down time during this period.				
3507	GOLD SPUTTERING SYS.	had no down time during this period.				
3508	ISOTHERMAL ANNEALER	had no down time during this period.				
3509	ASM NITRIDE DEP	had no down time during this period.				
3510	ASM OXIDE RECVD	had no down time during this period.				
4501	TOKUDA ETCHER #1	had no down time during this period.				
4502	ELECTROTECH A1 ETCHER	had no down time during this period.				
4503	TOKUDA ETCHER #2	had no down time during this period.				
4504	LFE RESIST ETCH	had no down time during this period.				
4505	LFE RESIST STRIP	had no down time during this period.				
4506	LFE RESIST STRIP	had no down time during this period.				
4507	LFE RESIST STRIP	had no down time during this period.				

B7 - WTS COMPUTER-GENERATED MAJOR STEP TRAVELLER

LOT TO : 5NM061502X DEVICE :
ASSIGNED BY : DATE : / /

MAJOR STEP # : 023.00

1023 METAL DEF MASK

MASK #40

[illegible]

51030 Coat/Bake

Coater ID#_____, Fgm "CNETL"

58001 Input Mask: Info

Serial# _____ Layer/Rev _____ / _____

S1051 Align Expose

Aligner#_____, Exp. Time_____

S1004 Develop

Wet Stat# 7 or #8, 60"

S1032 Hard Bake

Autofab Program METAL

S8123 Defect Density Ins

5pt./w, 4w, 20%-3w/bt, 1x

58105 Critical Dimension

1pt/wf, 3wf, OSI or Nanoline

DATA:

Waf #	Msk/Rev	Substr.	Pttrn	Exp.	Dev.	Align	Contam	Spin	Other
-------	---------	---------	-------	------	------	-------	--------	------	-------

[illegible]

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